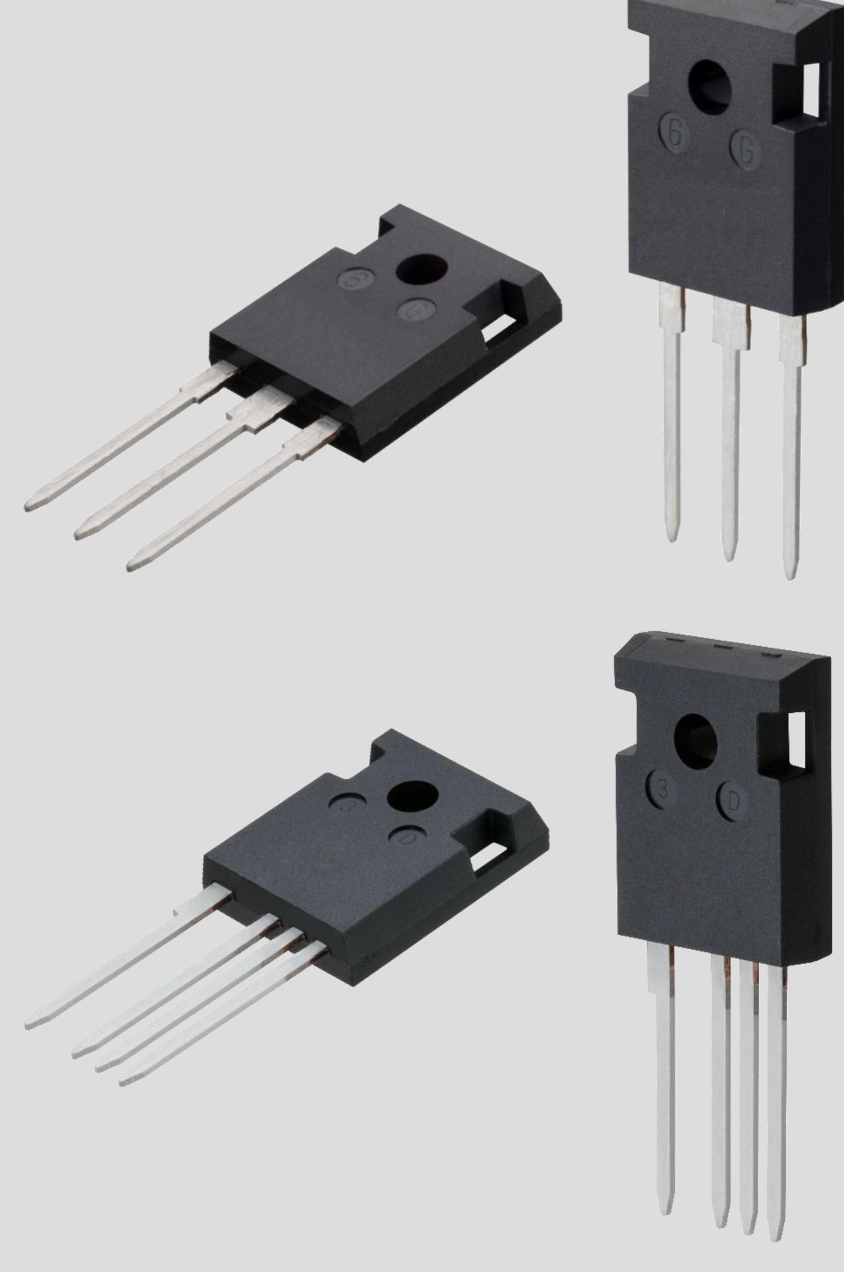

Discrete IGBT

Application Manual

Dec. 2025

Fuji Electric Co., Ltd.

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⚠Cautions

This manual contains the product specifications, characteristics, data, materials, and structures as of December 2025.
The contents are subject to change without notice for specification changes or other reasons. When using a product listed in this manual, be sure to obtain the latest specifications.

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Contents

Chapter 1 Structure and Features 1-1

1. History of IGBT Structure 1-2
2. Structure of Discrete IGBT 1-4
3. Circuit Configuration of Discrete IGBT 1-5
4. Features of TO-247-4 1-6
5. How to Read Discrete IGBT Product Part Number 1-9
6. Product Marking 1-10
7. RoHS Compliance 1-11

Chapter 2 Terms and Characteristics 2-1

1. Explanation of Terms 2-2
2. Characteristics of IGBT and FWD 2-5

Chapter 3 Discrete IGBT Selection and Application 3-1

1. Selection of Discrete IGBT 3-2
2. ESD Protection Measures 3-3
3. Work Environment 3-4
4. Gate Protection 3-5
5. Protection Circuits Design 3-5
6. Cooling Design 3-6
7. Gate Drive Circuits Design 3-6
8. Parallel Connection 3-6
9. Application of TO-247-4 3-7
10. Mounting Notes 3-8
11. Soldering 3-9
12. Cleaning 3-9
13. Terminal Processing and Mounting 3-10
14. Storage 3-11
15. Transportation 3-11
16. Precautions for Use 3-12

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Chapter 4 Typical Troubles and Troubleshooting 4-1
1. Troubleshooting 4-2
2. IGBT Test Procedures 4-7
3. Typical Troubles and Troubleshooting 4-9

Chapter 5 Protection Circuit Design 5-1
1. Short Circuit (Overcurrent) Protection 5-2
2. Overvoltage Protection 5-8

Chapter 6 Cooling Design 6-1
1. Power Loss of Discrete IGBT 6-2
2. About Fuji IGBT Simulator 6-3
3. Power Loss Calculation Method of Boost Chopper Circuit 6-4
4. Power Loss Calculation Method of 3-phase 2-level PWM Inverter Circuit 6-5
5. Concept of Cooling Design 6-9

Chapter 7 Gate Drive Circuit Design 7-1
1. IGBT Gate Drive Conditions and Main Characteristics 7-2
2. Drive Current 7-6
3. Setting Dead Time 7-7
4. Examples of Gate Drive Circuits 7-9
5. Precautions for Gate Drive Circuit Design 7-10

Chapter 8 Parallel Connections 8-1
1. Selection of Discrete IGBTs 8-2
2. Main Circuit Design 8-6
3. Gate Drive Circuit Design 8-8
4. Cooling Design 8-11

Chapter 9 Evaluation and Measurement 9-1
1. Evaluation and Measurement Methods 9-2
2. Voltage Measurement 9-3
3. Current Measurement 9-5

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Chapter 1 Structure and Features

1. History of IGBT Structure	1-2
2. Structure of Discrete IGBT	1-4
3. Circuit Configuration of Discrete IGBT	1-5
4. Features of TO-247-4	1-6
5. How to Read Discrete IGBT Product Part Number	1-9
6. Product Marking	1-10
7. RoHS Compliance	1-11

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The insulated gate bipolar transistors (IGBTs), applied to equipment such as variable-speed motor drives and uninterruptible power supplies for computers, are developing rapidly in response to the increasing demand for energy saving, weight reduction, and downsizing of equipment in recent years. The IGBT is a switching device designed to have the high-speed switching performance and gate voltage control of a power MOSFET as well as the high-voltage / large-current handling capability of bipolar transistor.

1. History of IGBT Structure

The n-channel IGBT, which forms a n-type inversion layer when positive voltage is applied to the gate, has a structure in which the n+ layer on the drain side of the power MOSFET is replaced with a p+ layer. It is a bipolar device that can reduce on-resistance at large current with conductivity modulation.

The IGBT structure can be roughly divided into the surface gate structure, the bulk structure that forms the n-drift layer, and the backside structure. There are two types of surface gate structures. One is the planar gate structure, in which the gates are formed on the wafer surface, namely the chip surface. The other is the trench gate structure, in which trenches are made to form the gates in the wafer. On the other hand, the bulk structure can be roughly divided into the punch-through type, in which the depletion layer reaches the collector side at turn-off, and the non-punch-through type, in which it does not reach the collector side. The comparison of the n-channel IGBTs is shown in Fig. 1-1.

Fuji Electric has been supplying IGBTs to the market since it commercialized them in 1988. The planar-gate punch-through IGBT was the mainstream IGBT at that time. The punch-through IGBT used the epitaxial wafer and low on-state voltage was achieved by injecting a large amount of minority carriers from the collector layer to obtain conductivity modulation effect. At the same time, the lifetime control technology was used because the excess carriers, which were high-injected into the n-drift layer, has to be removed quickly at turn-off. As a result, both low on-state voltage and low turn-off switching loss (E_{off}) were achieved. The lifetime control technology was widely used because it was relatively easy to apply into the IGBT manufacturing process. However, there were problems such as large variations in on-state voltage and the output characteristics showing negative temperature characteristics. Therefore, with the increasing capacity of IGBT modules and the power converters using them, the demand for IGBT characteristics that facilitate parallel connection has increased.

The non-punch-through IGBT was developed to overcome these issues. The non-punch-through IGBT controls the minority carrier injection efficiency by controlling the concentration of impurities in the collector (p-collector layer), and controls the internal electric field and transport efficiency by controlling the thickness and resistivity of the n-drift layer. The non-punch-through IGBTs use the FZ (Floating Zone) wafer instead of the epitaxial wafer. Therefore, the superiority of the FZ wafer compared to the epitaxial wafer can be reflected in the IGBT chip. For example, FZ wafers have less crystal defects and low internal stress, making it easy to manufacture high voltage chips of 1700V and above. In addition, the carrier lifetime of FZ wafers is very long, and the excess carrier distribution control of the IGBT chip only needs to consider minority carrier injection from the p-collector layer. Furthermore, variations in characteristics such as on-state voltage are greatly reduced.

On the other hand, in order to achieve a low on-state voltage, it was necessary to improve the transport efficiency. In particular, IGBT wafers with a withstand voltage of 1200V or less required a special manufacturing technology to thin the n-drift layer. Therefore, Fuji Electric has developed new technologies for production of thinner wafers and improved the characteristics.

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To further improve the characteristics, IGBTs with thinner chip thickness are required. However, the thickness of the n-drift layer constitutes most of the chip thickness, and if the thickness is too thin, the specified voltage cannot be maintained. The FS (Field Stop) structure solved this problem that hinder the improvement of the characteristics. In the FS structure, a high concentration FS layer is provided in the n-drift layer. This structure makes it possible to further reduce the thickness of the chip and improve its characteristics.

Fuji Electric has also advanced the miniaturization of the surface structure that is imperative to improve the characteristics of IGBT. The IGBT is formed by arranging many basic structures called cells. The higher the number of IGBT cells, the lower the on-state voltage will be. In order to increase cell density, the surface structure has changed from the planar structure, in which the IGBT cells are formed on the wafer surface two-dimensionally, to the trench structure, in which the trenches are formed on the wafer surface and the gates structure are formed three-dimensionally. In this way, Fuji Electric has improved the characteristics by applying various technologies to the bulk structure and the surface structure.

Gate Emitter P N+ N- drift N+ buffer P+ substrate PT-Epi Collector

Planar Gate

Gate Emitter P N+ N- drift NPT (Non Punch Through) P+ collector Collector

Emitter N+ P Gate Trench Gate N- drift Field-Stop N- field stop P+ collector Collector

(a) Punch-through type (b) Non-Punch-through type (c) Field Stop type

Fig. 1-1 Structure comparison of IGBT

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2. Structure of Discrete IGBT

Fig. 1-2 shows the structure of a TO-247 device that incorporates an IGBT and a FWD. Fig. 1-2(a) shows the external appearance, while Fig. 1-2(b) shows the internal structure. ①, ② and ③ correspond to the Gate, Collector, and Emitter terminals, respectively. Unlike typical IGBT modules, discrete IGBT does not have an insulating substrate.

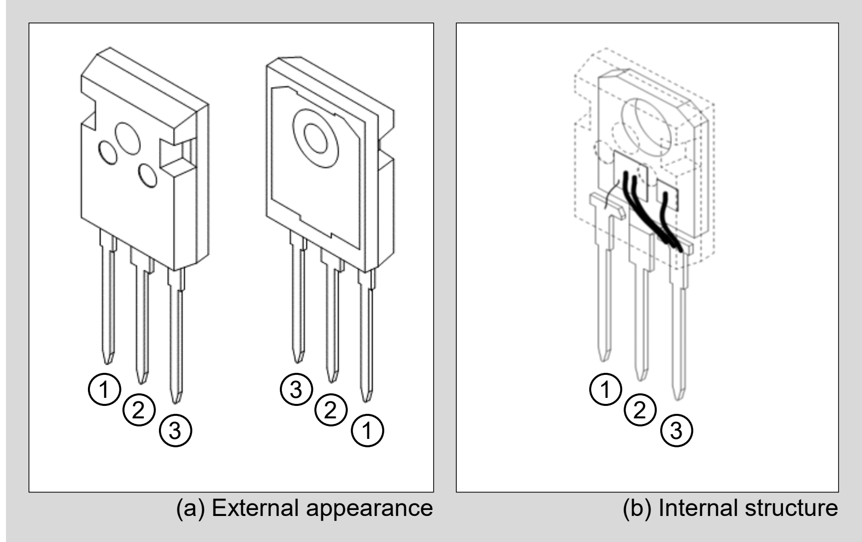

Fig. 1-2 Structure of a discrete IGBT

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3. Circuit Configuration of Discrete IGBT

Table1-1 shows the circuit configuration of the Discrete IGBT.

Table1-1 Circuit configuration of discrete IGBT

Package name	Appearance	Equivalent circuit	Features
TO-247			This product contains an IGBT and a FWD connected in anti-parallel. It is widely used in applications such as 2-level and 3-level PWM inverter circuits and chopper circuits.
			This product contains only IGBT. It is typically used in application where FWD is not required, such as in chopper circuit.
			This product contains an IGBT with reverse blocking voltage (RB-IGBT). It is used as a bidirectional switch such as the midpoint device in T-type NPC 3-level PWM inverter circuits.
TO-247-4			This product is a TO-247 package with an additional sub-Emitter terminal. Compared with the standard TO-247 package, it offers lower switching loss and reduced ringing of the gate-voltage. (refer to Section 4. “Features of TO-247-4” and Chapter 3 for details)

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4. Features of TO-247-4

In addition to the 3-terminal type TO-247 package shown in Fig. 1-3 (a), Fuji Electric also offers the 4-terminal type TO-247-4 package shown in Fig. 1-3 (b).

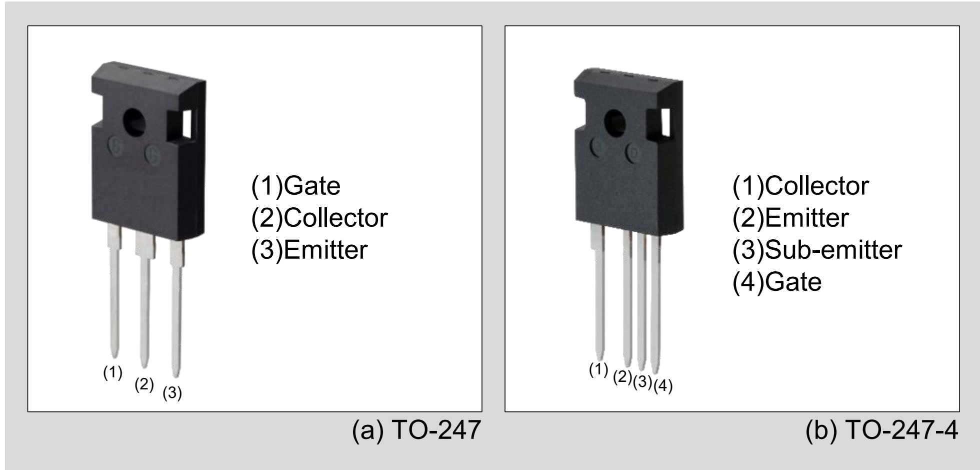

Fig. 1-3 Package appearance and terminal arrangement

In the 4-terminal TO-247-4 package, which adds an additional sub-emitter terminal, the common-emitter inductance LE can be separated from the gate drive circuit as shown in Fig. 1-4 (Kelvin connection). This configuration mitigates the induced voltage $-L_E \cdot dI_C/dt$ generated by the current loop in the gate drive path. As a result, compared with the conventional 3-terminal TO-247, the gate responds more quickly, switching loss are reduced (refer to Chapter 2 for details), and gate-voltage ringing is suppressed.

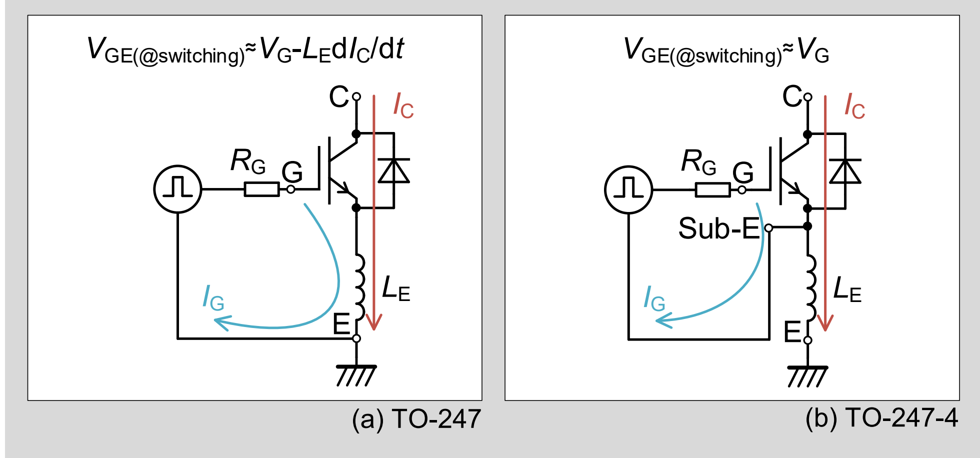

Fig. 1-4 Schematic diagram of internal circuit

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Fig. 1-5 and Fig. 1-6 compare the I_C dependence of the switching loss for the TO-247 device (FGW75XS120C) and TO-247-4 device (FGZ75XS120C). These figures show that the impact of the induced voltage $-L_E \cdot dI_C/dt$ is mitigated, resulting in lower switching loss.

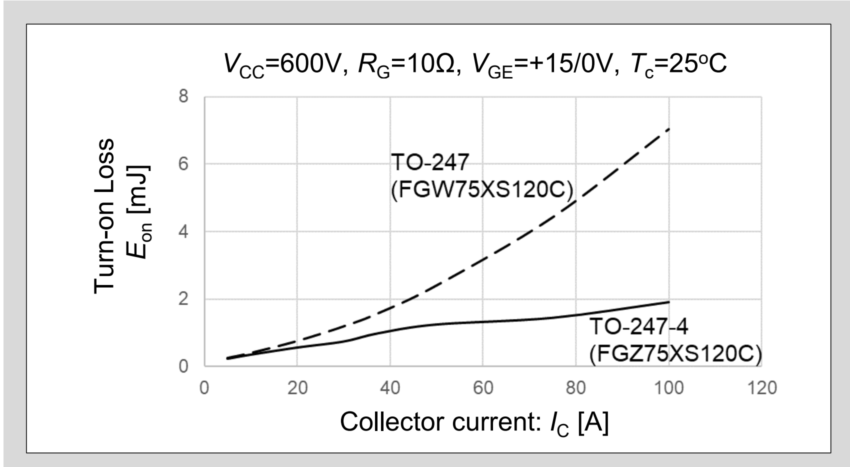

Fig. 1-5 TO-247 versus TO-247-4 turn-on loss

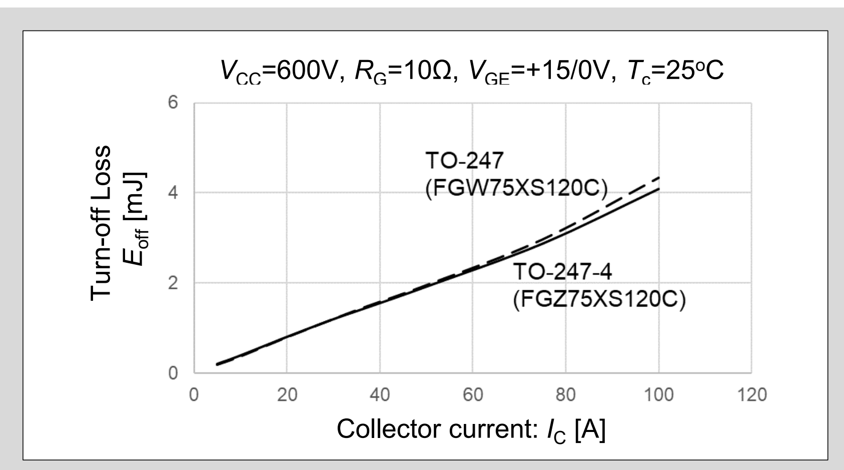

Fig. 1-6 TO-247 versus TO-247-4 turn-off loss

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The turn-off waveforms for TO-247(FGW75XS120C) and TO-247-4(FGZ75XS120C) are shown in Fig. 1-7. It can be seen that when the current is interrupted, the TO-247-4 package suppresses the V_{GE} ringing that is present with the conventional package. Keep in mind, however, that although the TO-247-4 package reduces the $-L_E \cdot dI_C/dt$ induced voltage, thereby lowering switching loss and mitigating ringing, it also makes the device switch faster. Consequently, the rate of change of collector current (dI_C/dt) becomes higher, and the turn-off surge voltage increases. For details, refer to Chapter 3.

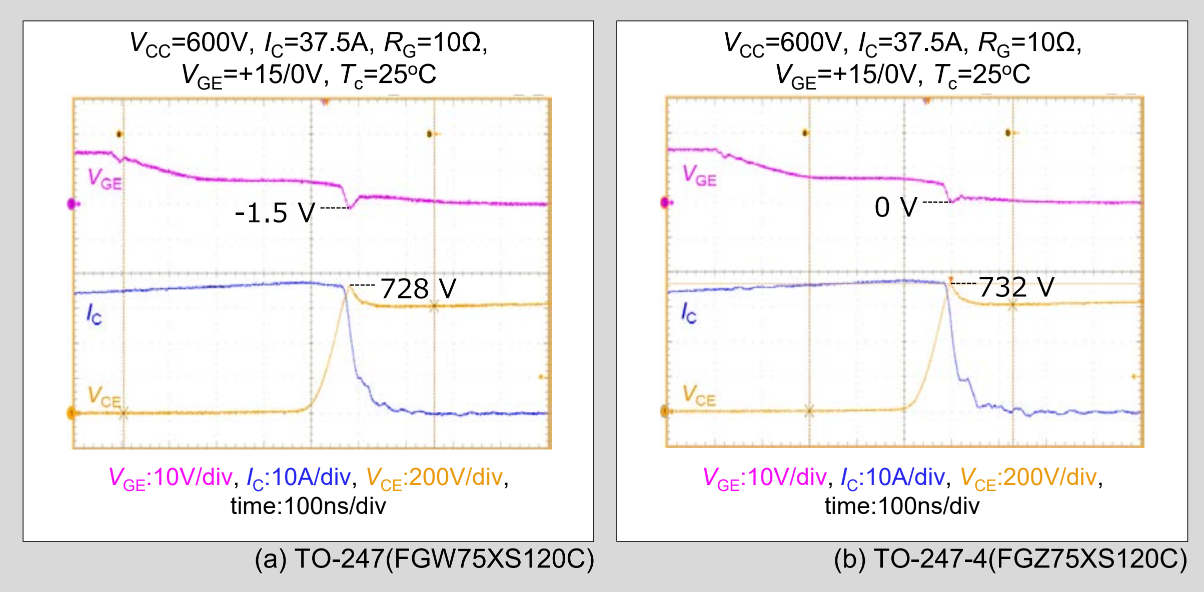

Fig. 1-7 Turn-off waveform comparison

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5. How to Read Discrete IGBT Product Part Number

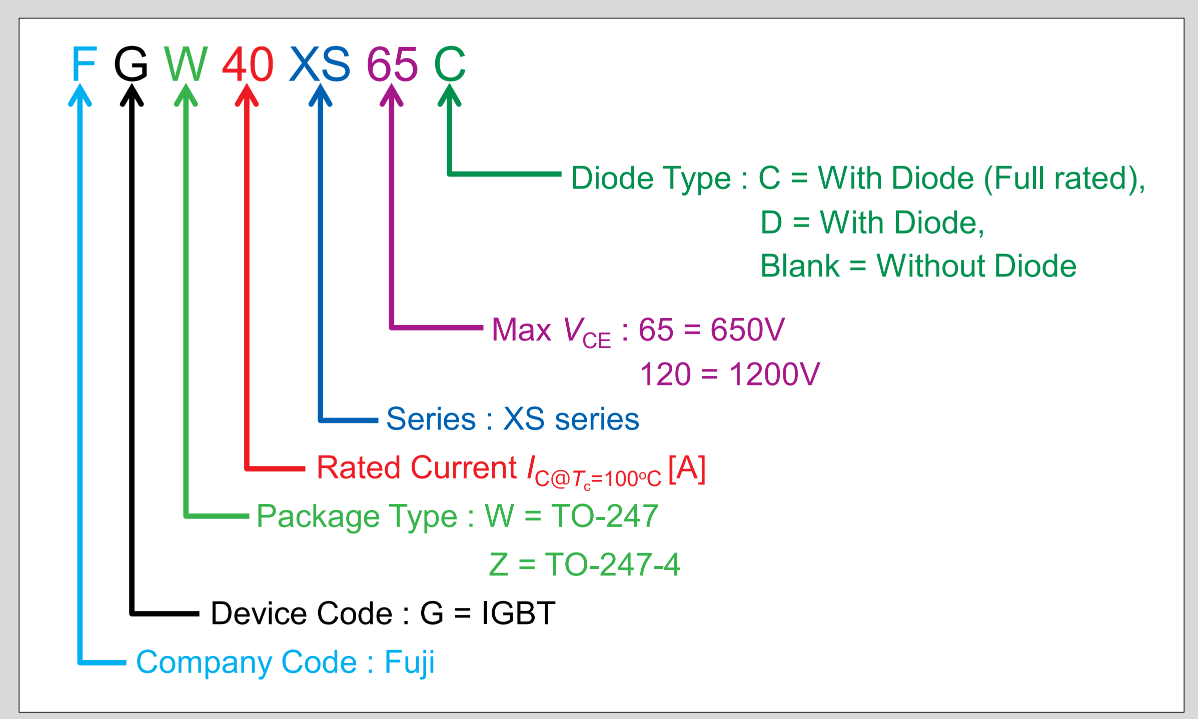

Fig. 1-8 XS series product part number

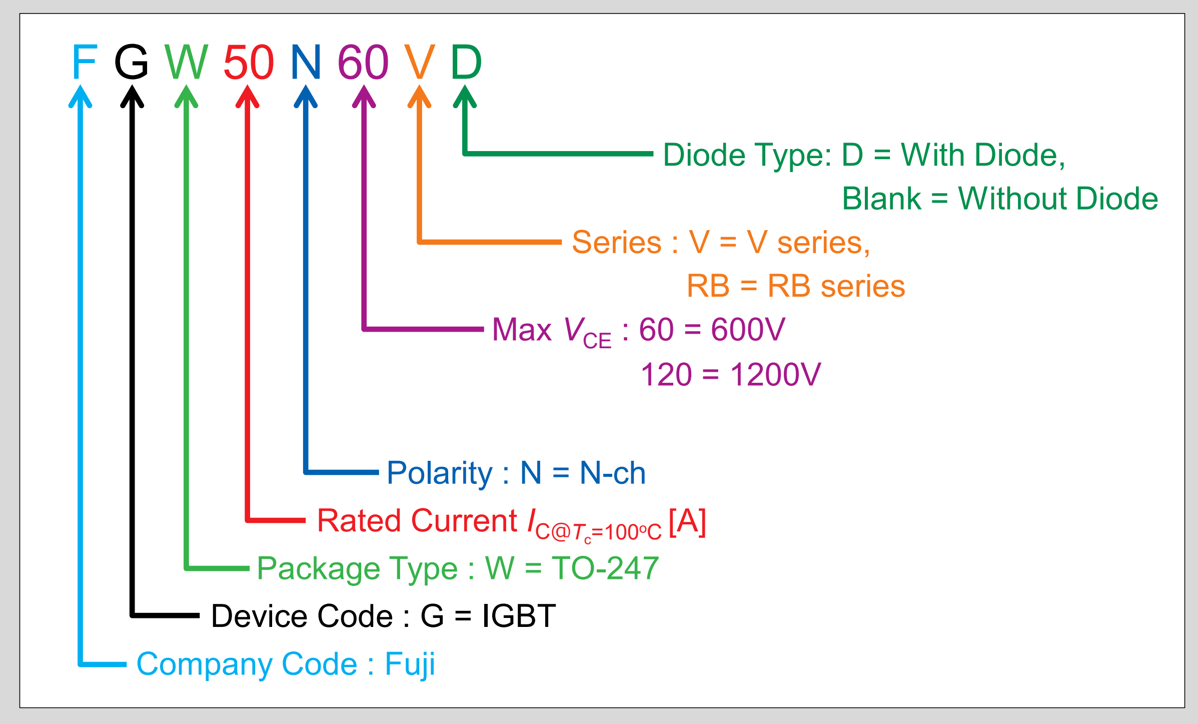

Fig. 1-9 V series product part number

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6. Product Marking

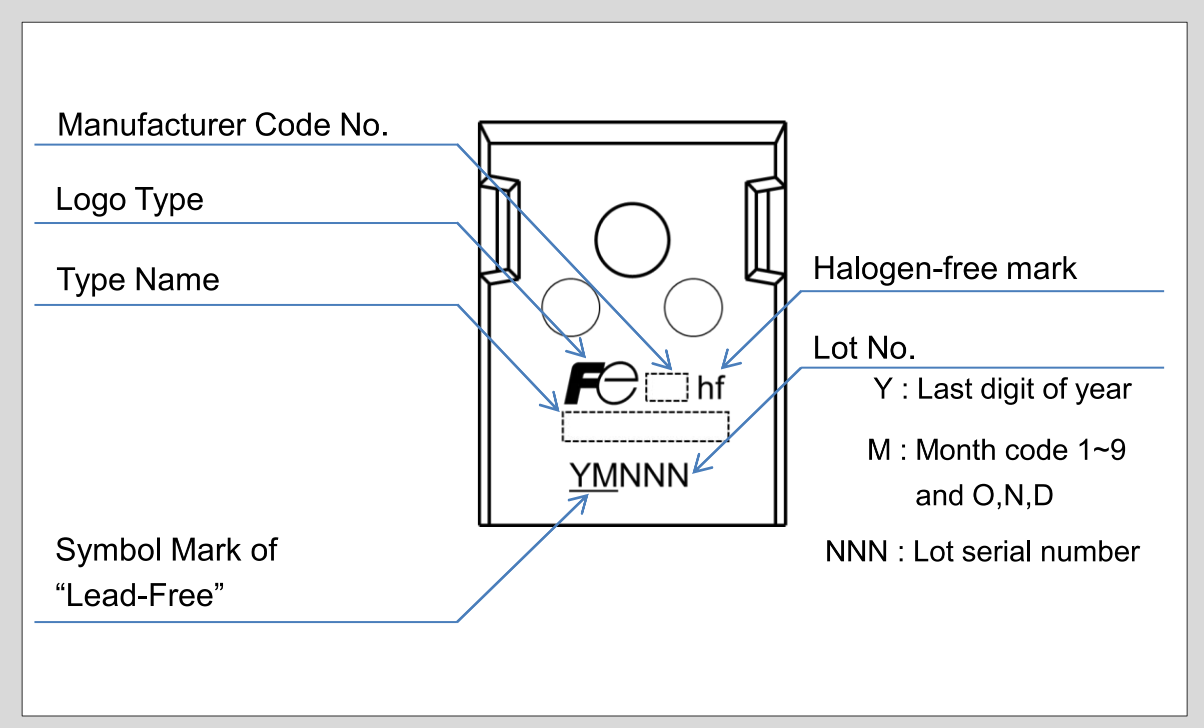

Fig. 1-10 Contents of the marking

Table 1-2 Example of marking

Series	Product part number	Type name
XS	FGW75XS120C	75XS120C
V	FGW40N120VD	40N120VD

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7. RoHS Compliance

The RoHS Directive (Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) is a regulation enacted by the European Union (EU) on July 1st, 2006, that restricts the use of specific hazardous substances in electrical and electronic equipment.

Under (EU) 2015/863, the ten restricted substances are:

- Pb (lead)
- Cd (cadmium)
- Cr^{6+} (hexavalent chromium)
- Hg (mercury)
- PBB (polybrominated biphenyls)
- PBDE (polybrominated diphenyl ethers)
- DEHP (bis(2-ethylhexyl) phthalate)
- BBP (benzyl butyl phthalate)
- DBP (dibutyl phthalate)
- DIBP (di-isobutyl phthalate)

Products containing any of these substances above the threshold levels (0.01 % for Cd; 0.1 % for all others) may not be sold within the EU, except for applications where substitution is technically impracticable and an exemption is granted.

Our discrete IGBT products are RoHS-compliant. The terminal solder plating uses lead-free solder (Pb < 0.1 %).

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Chapter 2 Terms and Characteristics

1. Explanation of Terms	2-2
2. Characteristics of IGBT and FWD	2-5

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This chapter describes the terms and characteristics of Discrete IGBTs.

1. Explanation of Terms

Various terms used in the data sheets of XS Series are explained below. Refer to the specifications for details.

Table 2-1 Absolute Maximum Ratings

Term	Symbol	Definitions and explanations (Refer to the specifications of each product for the conditions)
Collector-Emitter voltage	V_{CES}	Maximum Collector-Emitter (hereinafter referred to as C-E) voltage with Gate-Emitter (G-E) shorted.
Gate-Emitter voltage	V_{GES}	Maximum G-E voltage with C-E shorted.
Collector current	$I_{C@25}$	Maximum DC collector current of IGBT at T_c=25°C.
	$I_{C@100}$	Maximum DC collector current of IGBT at T_c=100°C.
	I_{CP}	Maximum pulse collector current of IGBT.
Diode forward current	$I_{F@25}$	Maximum DC forward current of FWD at T_c=25°C.
	$I_{F@100}$	Maximum DC forward current of FWD at T_c=100°C.
	I_{FP}	Maximum pulse forward current of FWD.
Collector power dissipation	P_{tot_IGBT}	Maximum power dissipation of IGBT at T_c=25°C.
FWD power dissipation	P_{tot_FWD}	Maximum power dissipation of FWD at T_c=25°C.
Operating virtual junction temperature	T_{vj}	Maximum junction temperature at which the device can operate without abnormalities. (The equipment must be designed so that this value is not exceeded under worst-case conditions.)
Storage temperature	T_{stg}	Temperature range for storage or transportation without being subjected to electrical load.

Note 1: Values at T_C = 25 °C unless otherwise specified

Note 2: The values listed as maximum ratings should not be exceeded under any circumstances.

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Table 2-2 Static electrical characteristics

Term	Symbol	Definitions and explanations (Refer to the specifications of each product for the conditions
Zero gate voltage collector current	I_{CES}	Collector current when a specific voltage is applied between C-E with G-E shorted.
Gate-Emitter leakage current	I_{GES}	Gate current when a specific voltage is applied between G-E with C-E shorted.
Gate-Emitter threshold voltage	$V_{GE(th)}$	G-E voltage (V_{GE}) at a specified I_C and C-E voltage.
Collector-Emitter saturation voltage	$V_{CE(sat)}$	C-E voltage at a specified collector current and G-E voltage.

Table 2-3 Dynamic electrical characteristics

Term	Symbol	Definitions and explanations (Refer to the specifications of each product for the conditions
Input capacitance	C_{ies}	G-E capacitance when a specified voltage is applied between G-E and C-E while C-E is shorted in AC.
Output capacitance	C_{oes}	C-E capacitance when a specified voltage is applied between G-E and C-E while G-E is shorted in AC.
Reverse transfer capacitance	C_{res}	C-G capacitance when a specified voltage is applied between G-E and C-E while G-E and C-E are shorted in AC.
Gate charge	Q_G	Amount of charge required to turn-on the IGBT.
Turn-on delay time	$t_{d(on)}$	The time during IGBT turn-on when V_{GE} reaches 10% of its maximum value until collector current reaches 10% of its maximum value. (see Fig. 2-3)
Rise time	t_r	The time during IGBT turn-on when collector current rises from 10% to 90% of its maximum value. (see Fig.2-3)
Turn-off delay time	$t_{d(off)}$	The time during IGBT turn-off when V_{GE} drops from 90% of its maximum value until collector current drops to 90% of its maximum value. (see Fig. 2-3)
Fall time	t_f	The time during IGBT turn-off when collector current drops from 90% to 10% of its maximum value. (see Fig. 2-3)
Turn-on loss	E_{on}	Switching loss generated during IGBT turn-on. (see Fig. 2-3)
Turn-off loss	E_{off}	Switching loss generated during IGBT turn-off. (see Fig. 2-3)

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Table 2-4 FWD characteristics

Term	Symbol	Definitions and explanations (Refer to the specifications of each product for the conditions
Forward voltage	V_F	Forward voltage of FWD at a specified forward current.
Diode reverse recovery time	t_{rr}	The time during FWD turn-off when the reverse recovery current crosses 0A until it recovers to 10% of the reverse recovery peak current. (see Fig. 2-4)
Diode reverse recovery charge	Q_{rr}	Amount of charges calculated as the time integral value of the reverse recovery current of FWD.

Table 2-5 Thermal resistance characteristics

Term	Symbol	Definitions and explanations (Refer to the specifications of each product for the conditions
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Thermal resistance between the chip (junction) and ambient without heat sink attached and windless.
Thermal resistance, IGBT junction to case	$R_{th(j-c)_IGBT}$	Thermal resistance between the chip (junction) and case of IGBT.
Thermal resistance, FWD junction to case	$R_{th(j-c)_FWD}$	Thermal resistance between the chip (junction) and case of FWD.

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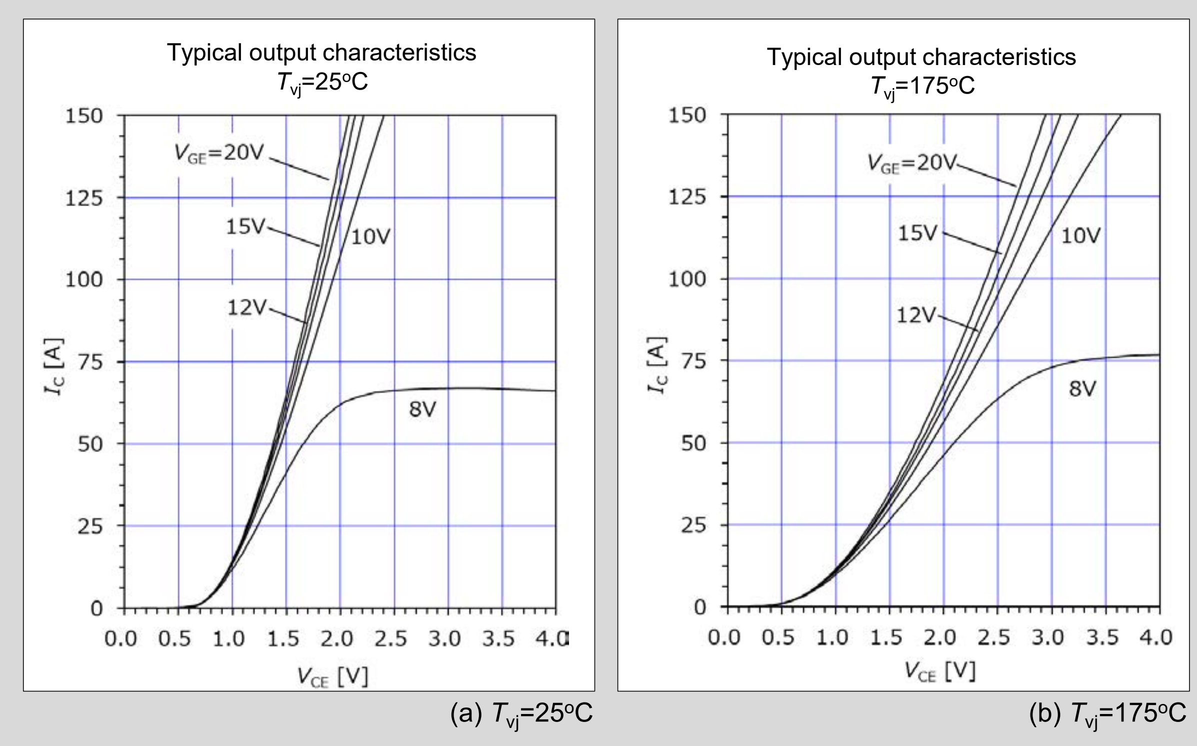
2. Characteristics of IGBT and FWD

Discrete IGBT products are available in two types: products with antiparallel FWD, and products with only IGBT. Using FGZ75XS120C (1200V/75A device) as an example, the various characteristics of IGBT and FWD described in the specifications are explained below.

2.1 Static characteristics

Fig. 2-1 shows the V_{GE} dependence of V_{CE} - I_C characteristics (output characteristics). These curves show the relationship between V_{CE} and I_C when the IGBT is on, and it directly relates to the on-state power loss in the IGBT. Accordingly, the lower the V_{CE}, the smaller the power loss. Because this characteristic varies with virtual junction temperature T_{vj} and gate-emitter voltage V_{GE}, it is necessary to take both into account when designing your equipment.

As a general guideline, we recommend to operate the IGBT at V_{GE}=15V, and the equipment's maximum output peak current lower than the device's rated current.



(a) T_{vj}=25°C (b) T_{vj}=175°C

Fig. 2-1 V_{CE} - I_C characteristics

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2.2 Switching characteristics

Since IGBTs are generally used in switching applications, it is important to thoroughly understand their turn-on and turn-off switching characteristics. Because these characteristics vary with a number of parameters, it is necessary to take them into account when designing your system.

Switching characteristics can be broadly divided into switching times and switching loss. These characteristics are measured using the test circuit shown in Fig. 2-2.

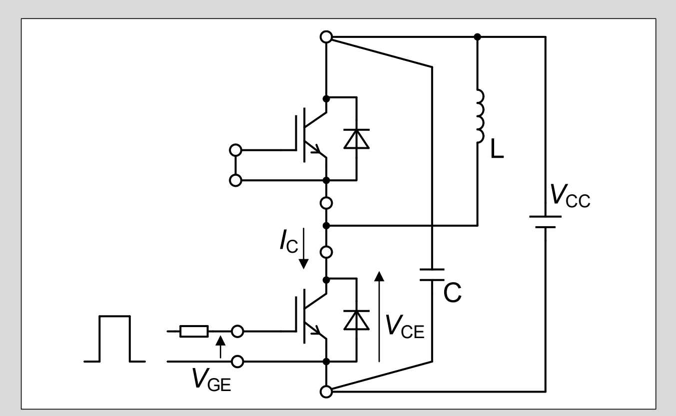

Fig. 2-2 Switching characteristics measuring circuit

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Fig. 2-3 and Fig. 2-4 show the definitions of the characteristics $t_{d(on)}$, t_r, $t_{d(off)}$, t_f, E_{on}, E_{off}, and t_{rr} in Table 2-3 and Table 2-4, as well as the definitions of E_{rr} and I_{rr}.

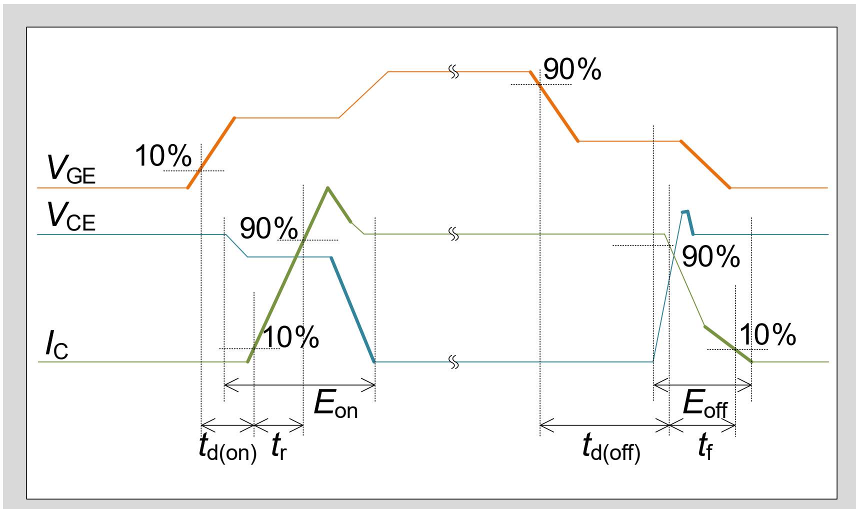

Fig. 2-3 Definition of switching time (turn-on and turn-off waveforms)

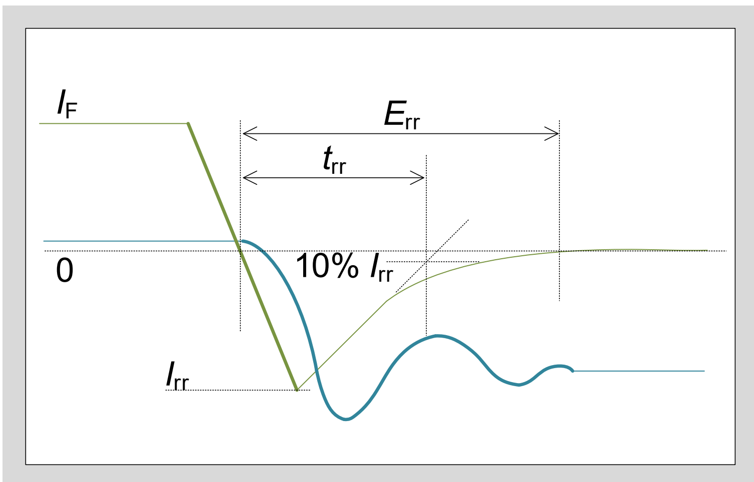

Fig. 2-4 Definition of switching time (reverse-recovery waveform)

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Fig. 2-5 shows the relationship between these switching times and the collector current I_C. Fig. 2-6 shows how the switching times vary with gate resistance R_G. Because switching times varies depending on I_C, virtual junction temperature T_{vj} and R_G, it is necessary to take these parameters into account when designing your equipment.

For example, when operating under conditions that increase switching times such as $t_{d(off)}$ or t_f, insufficient dead time can lead to series arm short circuit (refer to Chapter 4 for details), potentially destroying the device. Conversely, if switching times such as t_f is too short, the transient current change rate dI_C/dt will becomes high, causing an excessive surge voltage (=L_S·dI_C/dt) from the circuit stray inductance. Since this surge voltage is superimposed on the applied voltage, it can push the device beyond its RBSOA (refer to Chapters 2 and 4 for details), risking device failure.

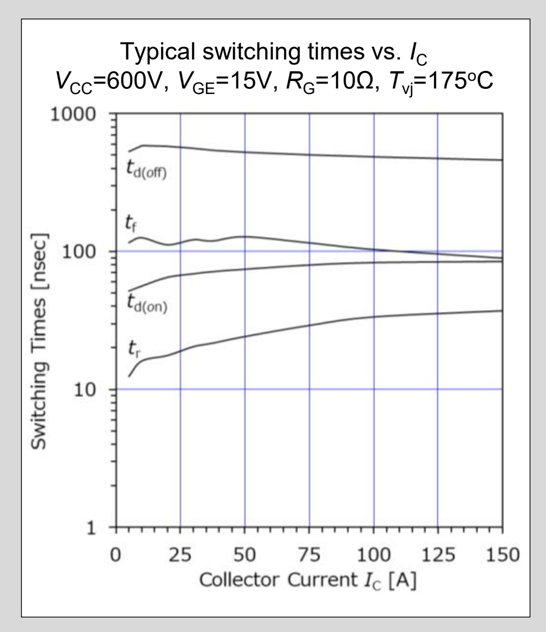

Fig. 2-5 Switching time - I_C characteristics

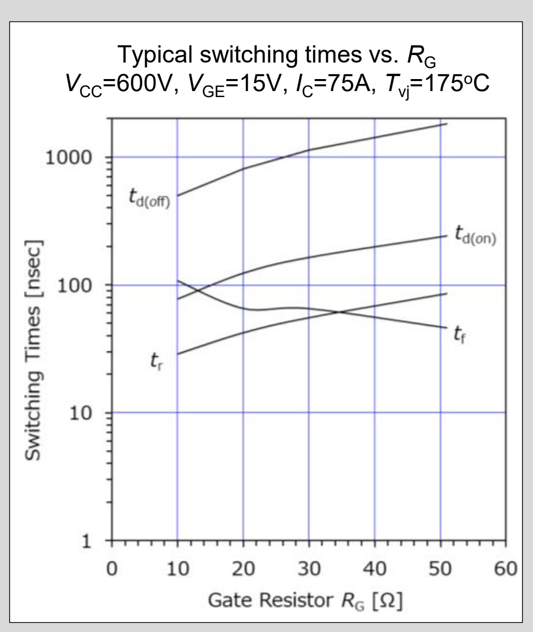

Fig. 2-6 Switching time - R_G characteristics

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Switching loss (E_{on}, E_{off}, E_{rr}) occurs every time an IGBT is turned on or off, therefore it is important to minimize this loss as much as possible. As shown in Fig. 2-7, 2-8 and 2-9, switching loss changes in accordance with I_C, T_{vj}, and R_G. In particular, the selection of R_G is important. If it is too large, the switching loss will increase, and series arm short circuit due to the aforementioned insufficient dead time will easily occur. Conversely, if R_G is reduced to reduce switching loss, the aforementioned excessive surge voltage ($=L_S \cdot dI_C/dt$) may occur.

The value of main circuit inductance L_S has great influence on R_G selection. The smaller the value is, the smaller the surge voltage will be, making it easier to consider R_G selection. Therefore, it is recommended to design the L_S value as small as possible.

When selecting R_G, it is also necessary to consider matching with the capacitance of the IGBT drive circuit. Therefore, please select the R_G after careful consideration using the capacitance characteristics as shown in Chapter 2.3.

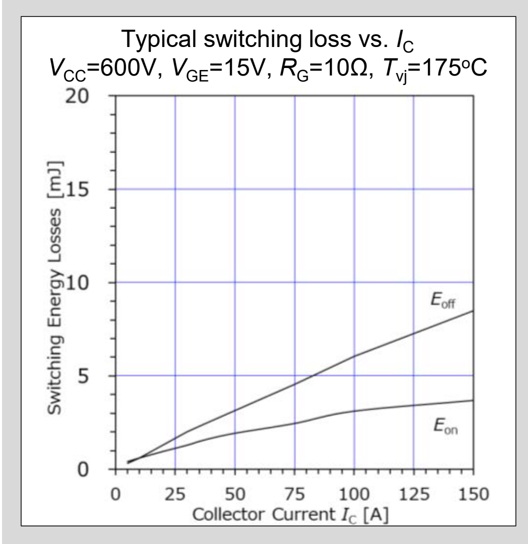

Fig. 2-7 E_{on}, E_{off} – I_C characteristics

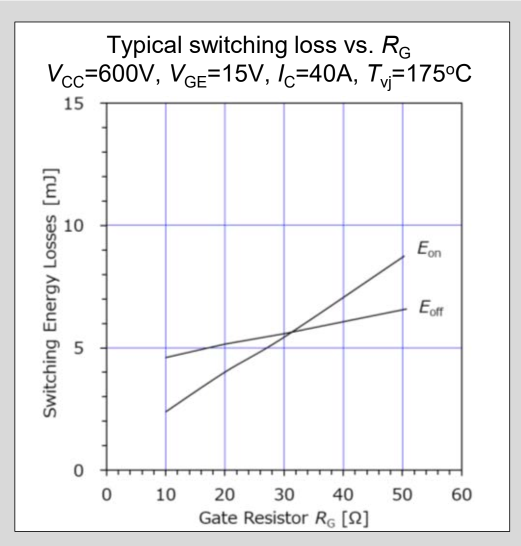

Fig. 2-8 E_{on}, E_{off} – R_G characteristics

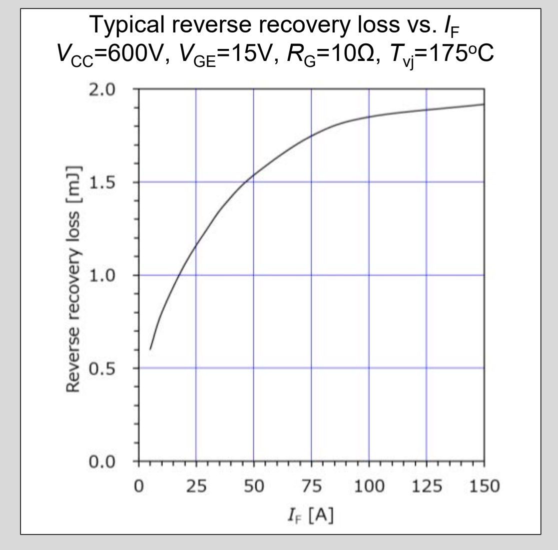

Fig. 2-9 E_{rr} – I_F characteristics

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2.3 Capacitance characteristics

Fig. 2-10 shows the characteristics of gate charge Q_g. This characteristic shows the change of V_{GE} with respect to Q_g. An increase in Q_G corresponds to charging the G-E capacitance of the IGBT; as Q_G rises, V_{GE} (= Q_G divided by the G–E capacitance) increases until the IGBT turns on. Once on, V_{CE} falls to the saturation voltage. In this way, Q_G indicates the total charge required to drive the IGBT. Use this characteristic when determining the power supply capacity of the gate-drive circuit.

Fig. 2-11 shows the characteristics of the IGBT's junction capacitances. The specific capacitances C_{ies}, C_{oes} and C_{res} are shown in Fig. 2-12. Use these capacitance characteristics together with the Q_G characteristic when designing your gate drive circuit.

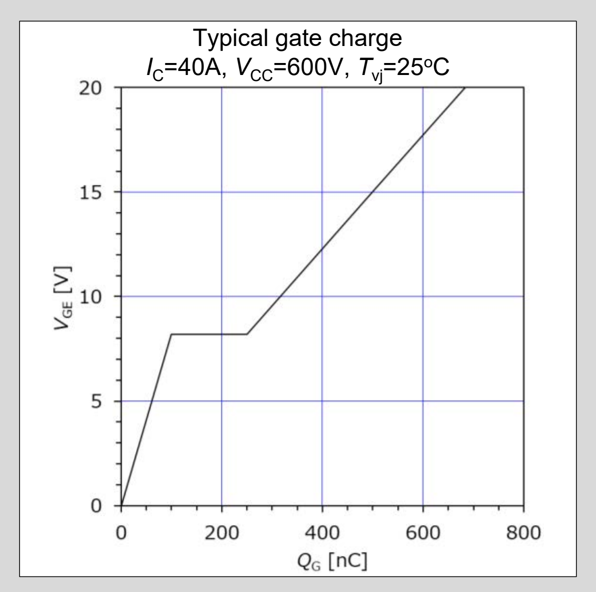

Fig. 2-10 V_{GE} - Q_g characteristics

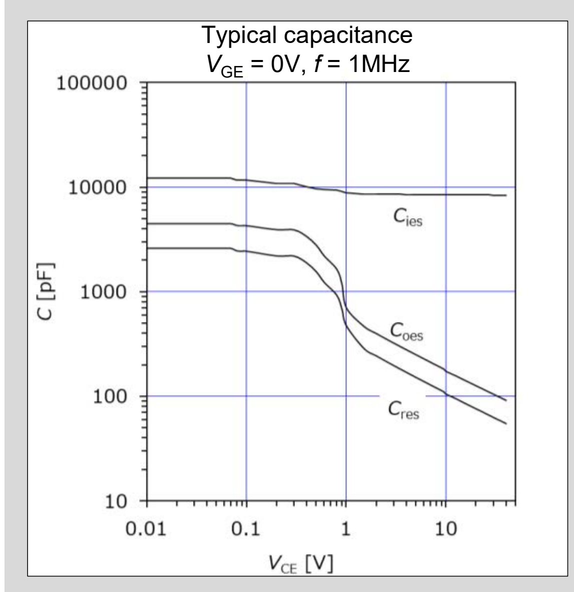

Fig. 2-11 Junction capacitance characteristic

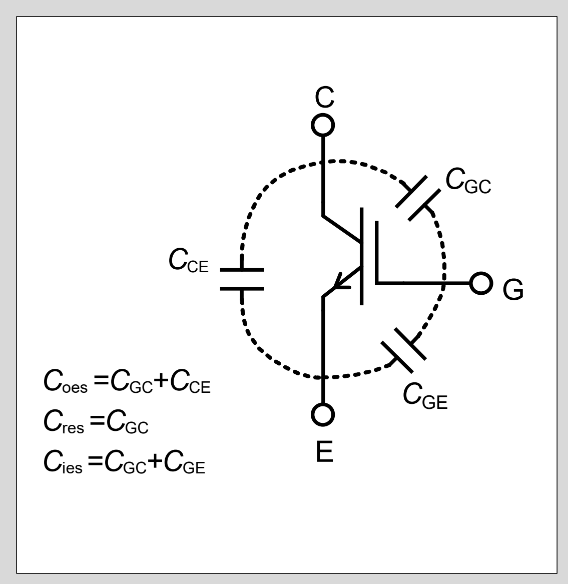

Fig. 2-12 Junction capacitance

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2.4 Reverse bias safe operating area

During turn-off, IGBT has a safe operating area defined by V_{CE} and I_C called RBSOA (Reverse Bias Safe Operating Area). Fig. 2-14 shows the area of RBSOA. The operating locus of V_{CE} - I_C at turn-off must be designed to fall within this RBSOA area.

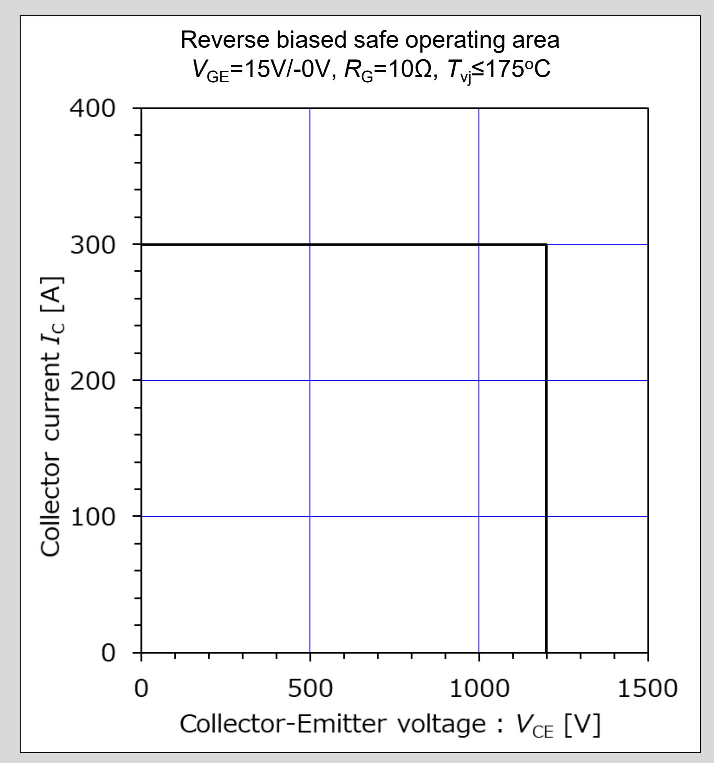

Fig. 2-13 RBSOA

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2.5 FWD characteristics

In discrete IGBTs with built-in antiparallel FWD, the FWD has V_F – I_F characteristic shown in Fig. 2-14, the reverse-recovery characteristic (t_{rr}, Q_{rr}) shown in Fig. 2-15, and the E_{rr} characteristic shown in Fig. 2-9. Use these characteristics to calculate the power loss of the FWD as well as the IGBT. Note that FWD characteristics vary in accordance with I_F, T_{vj}, R_G, etc.

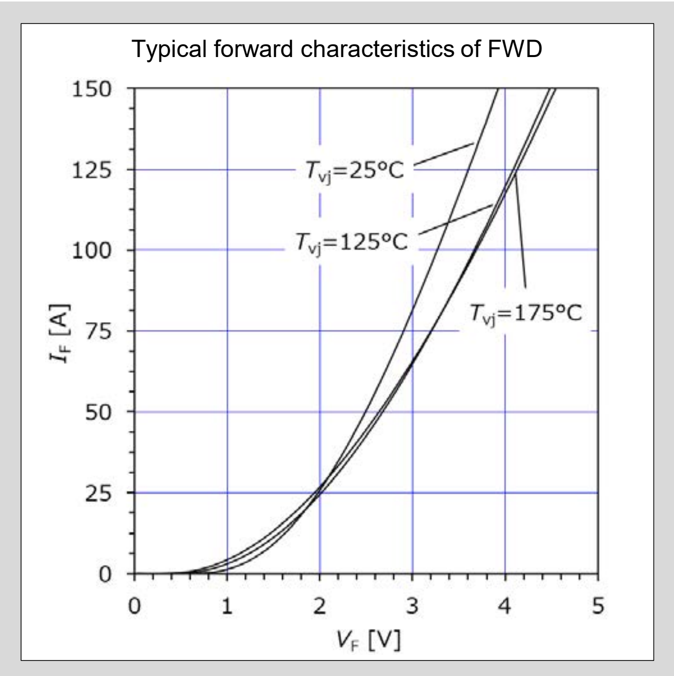

Fig. 2-14 V_F - I_F characteristics

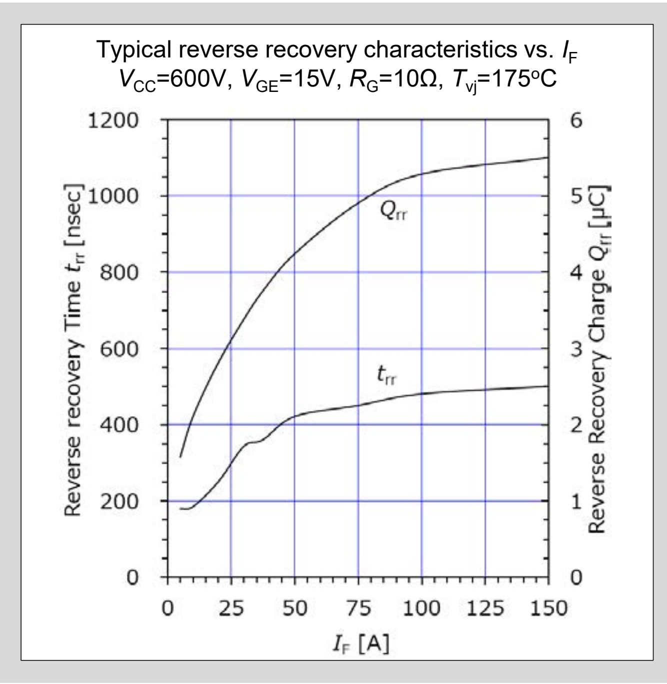

Fig. 2-15 t_{rr}, Q_{rr} characteristics

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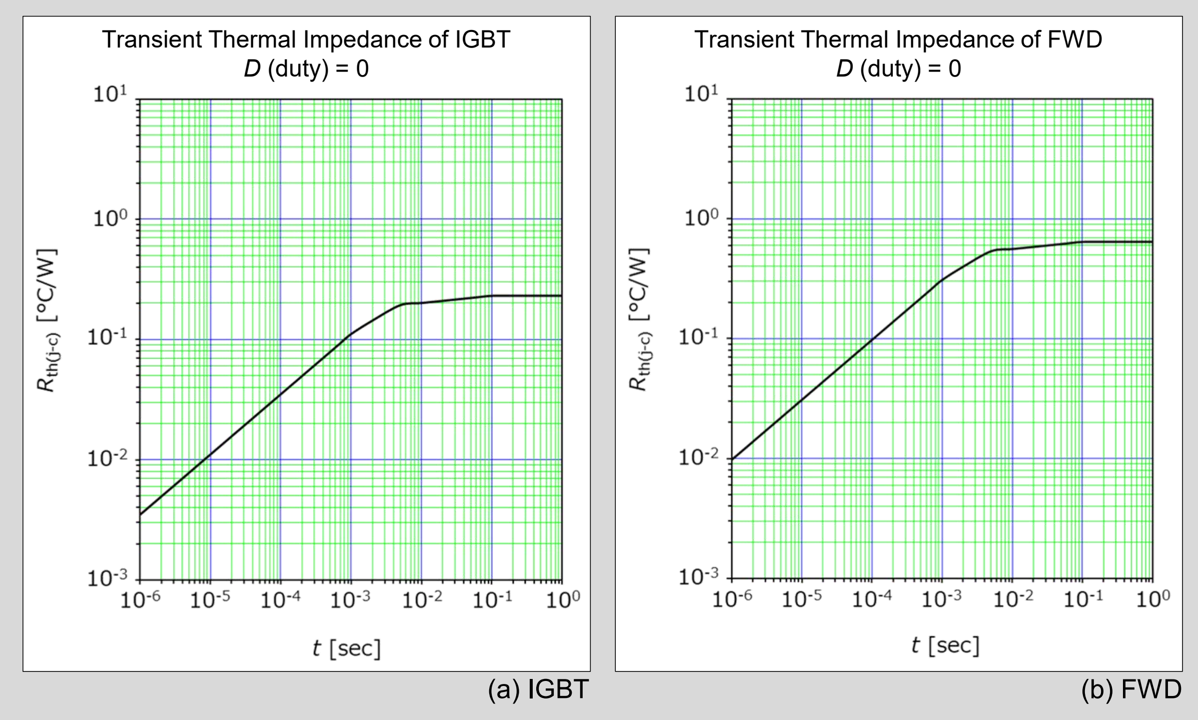
2.6 Transient thermal impedance characteristics

Fig. 2-16 shows the transient thermal impedance characteristics used for calculating temperature rise and designing the heat sink. These transient thermal impedance characteristics are used to calculate the T_{vj} of IGBTs and FWDs. (For details, refer to Chapter 6, “Cooling Design”)



(a) IGBT (b) FWD

Fig. 2-16 Transient thermal impedance characteristics

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Chapter 3 Discrete IGBT Selection and Application

1.	Selection of Discrete IGBT	3-2
2.	ESD Protection Measures	3-3
3.	Working Environment	3-4
4.	Gate Protection	3-5
5.	Protection Circuits Design	3-5
6.	Cooling Design	3-6
7.	Gate Drive Circuits Design	3-6
8.	Parallel Connection	3-6
9.	Application of TO-247-4	3-7
10.	Mounting Notes	3-8
11.	Soldering	3-9
12.	Cleaning	3-9
13.	Terminal Processing and Mounting	3-10
14.	Storage	3-11
15.	Transportation	3-11
16.	Precautions for Use	3-12

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This chapter describes the precautions when using discrete IGBT and application.

1. Selection of Discrete IGBT

When using discrete IGBTs, it is important to select products with the voltage and current ratings most suited for the intended application.

1.1 Voltage ratings

The voltage rating of a discrete IGBT is determined by the commercial power supply voltage of the equipment in which it is applied and the equipment’s DC link voltage. This relationship is shown in Table 3-1. Refer to the table when selecting a device for your application.

Table 3-1 Discrete IGBT voltage rating application example

	IGBT rated voltage	
	650V	1200V
Commercial power supply voltage	～240VAC	～480VAC
DC link voltage	～520VDC	～960VDC

1.2 Current rating

When the collector current I_C of the IGBT increases, both the conduction loss and switching loss increase, resulting in an increase in the device temperature. The virtual junction temperature T_{vj} of the IGBT and FWD must remain below the maximum limit, so choose a current rating that ensures T_{vj} never exceeds its specified maximum rating. Incorrect selection of current rating may lead to device destruction or deterioration of reliability.

Note that in high frequency switching applications, switching loss increases, which increases the device temperature. A common rule of thumb is to select a device which current rating is at least 2~3 times of the operating current. However, the selection of the current rating depends on the operating conditions and heat dissipation conditions of the equipment, thus it is important to select the current rating after checking the power loss and temperature rise in the equipment.

1.3 Maximum rating

Use the device within the maximum ratings (voltage, current, temperature, etc.) described in the specifications. Using the product beyond the maximum rating may destroy the device. Also, the value described in each item of the absolute maximum rating is specified for that item, not for combination of more than one item.

Even if the device is used within the maximum rating, factors such as ambient temperature and operating environment can shorten the product’s lifetime. Refer to the absolute maximum ratings, and evaluate and verify the compatibility of the device with the system or equipment.

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1.4 RBSOA

Make sure that the IGBT turn-off voltage and current operating locus are within the RBSOA specifications. Using the IGBT beyond the RBSOA region may destroy the device.

2. ESD Protection Measures

Although IGBTs have much higher ESD immunity than small-signal MOSFETs or integrated circuits, they can still be destroyed by static discharges.

As shown in Fig. 3-1, static charge on conductive objects can be safely removed by properly using conductive table mats, wrist straps, and floor mats. The speed at which the charge is discharged depends on the resistance of the discharge path and the capacitance of the charged object. Fig. 3-2 shows the equivalent circuit for a charged conductor with capacitance C and path resistance R. The voltage on the charged object as a function of time is given by the following equation.

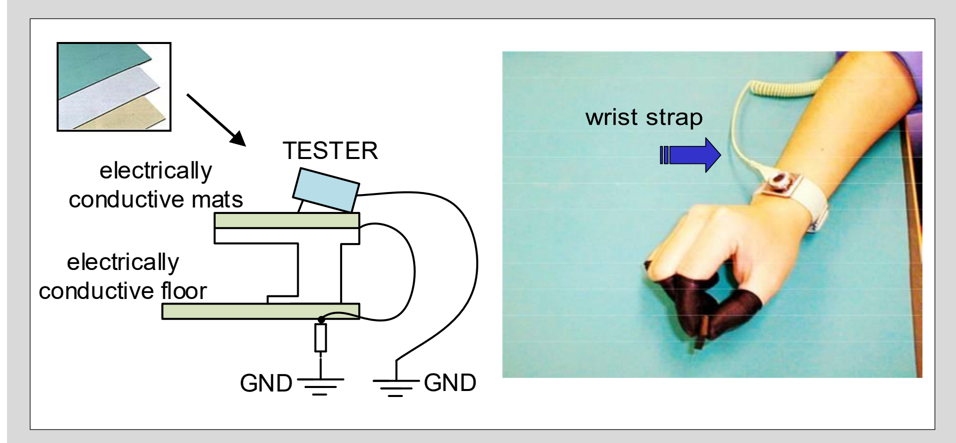

Fig. 3-1 Example of ESD protection measures

$$V(\mathrm{t}) = V_0 \cdot \exp\left(-\frac{t}{RC}\right)$$

V : Voltage of charged object at time t [V]
V_0 : Initial voltage of charged object [V]
t : Time [sec]
C : Capacity of charged object [F]
R : Resistance of discharge path [Ω]

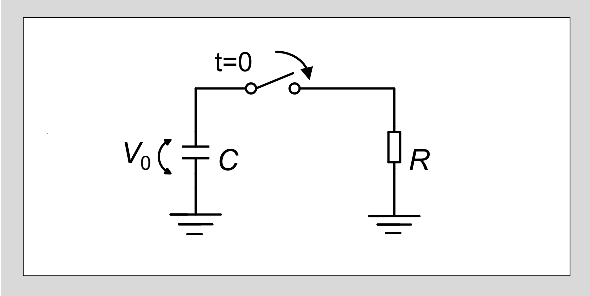

Fig. 3-2 Equivalent circuit of ESD discharge

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<Example>

This example shows how to calculate the required resistance to reduce a worker's static electricity to 100V or less in one second.

V = 100V (safe voltage)、V_0 = 10kV (initial voltage of the human body or charged object)、
t = 1s (maximum allowable time to achieve the safe voltage of 100V)、
C = 200pF (average human body capacitance, 100pF～400pF),
R = maximum allowable resistance to ground [Ω]

Substituting these values into the formula,

$$100 = 10 \times 10^3 \cdot \exp\left(-\frac{1}{200 \times 10^{-12} \cdot R}\right)$$

Therefore, $R \cong 1.09 \times 10^9 \Omega$ = 1090MΩ. If the resistor from the table mat, floor, or the wrist strap to ground is 1000MΩ or less, the voltage is discharged to the safety voltage of 100V in less than 1 second.

3. Working Environment

- Workers must be body-grounded. Wear a wrist strap, copper ring or similar device, and connect it to the ground with a resistance of about 1MΩ.
- Equip the workspace with conductive floor mats and/or table mats, all grounded. Also, maintain appropriate humidity.
- When using measuring instruments such as curve tracers, ground the instruments as well.
- When soldering, connect the soldering iron and solder bath to ground so that any leakage voltage from them cannot be applied to the discrete IGBTs.
- Do not touch the terminals directly, always handle the device by its package body.

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4. Gate Protection

Applying a voltage between the gate and emitter (G–E) that exceeds the absolute maximum rating can destroy the gate structure of the IGBT. Do not apply any voltage across G–E beyond its absolute maximum rating.

If the G–E path is open (i.e. the gate is floating) while a voltage is applied between the collector and emitter (C–E), the IGBT can also be damaged. This is due to a change in the collector potential induces a leakage current i (see Fig. 3-3) from the collector to the gate. This raises the gate potential, inadvertently turns the IGBT on, allows collector current I_C to flow, and causes the device to heat up and fail.

In practice, after you have installed a discrete IGBT into your equipment, a failure or malfunction in the gate drive circuit that leave the gate floating while the main circuit voltage is applied may destroy the IGBT for the reasons above (refer to Chapter 7, section 5.2). To prevent this, we recommend connecting a resistor R_{GE} of about 10 kΩ between gate and emitter.

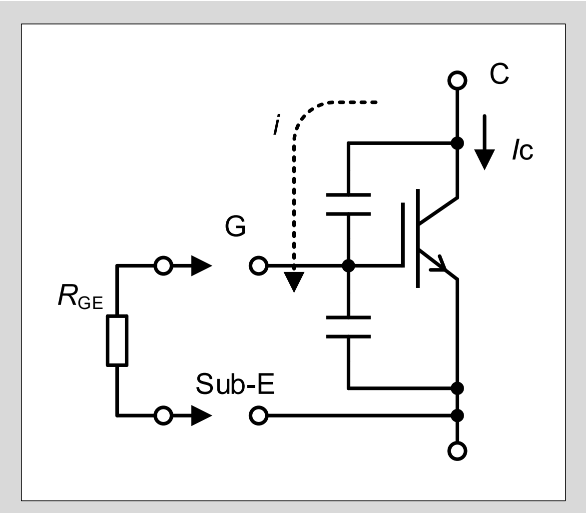

Fig. 3-3 IGBT behavior when G-E is open

5. Protection Circuits Design

Discrete IGBTs can be destroyed by abnormal conditions such as overcurrent or overvoltage. Therefore, it is critically important to design protection circuits that safeguard the device under those conditions. When designing a protection circuit for a discrete IGBT, you must fully understand the IGBT's characteristics (switching speeds, capacitances, thermal limits, etc.) and match the protection circuit's response (timing, thresholds, energy absorption capability) to those device characteristics.

If the protection circuit is not properly matched, the IGBT may still fail even though a protection circuit is present. Common examples of mismatches include:

- Overcurrent protection with too long turn-off delay, allowing excessive energy to flow before cutoff.
- Snubber circuits with capacitances that are too small, resulting in excessive surge voltages.

Detailed methods for overcurrent and overvoltage protection are provided in Chapter 5, "Protection Circuit Design Methods." Please refer to that chapter for design guidelines and examples.

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6. Cooling Design

Discrete IGBT have a maximum virtual junction temperature ($T_{vj(max)}$). An appropriate heat sink must be selected to keep the temperature below this value. When designing heat sink, the operating conditions of the Discrete IGBT has to be fully considered.

To perform the cooling design, first calculate the loss generated in the device, and based on those loss select a heat sink that keeps the temperature below the allowable limit. If the cooling design is insufficient, the junction temperature (T_{vj}) may exceed the maximum guaranteed temperature during actual operation, leading to device failure.

For detailed explanations and precautions, refer to Chapter 6, “Cooling Design”

7. Gate Drive Circuit Design

To fully realize the device’s performance, the design of the gate drive circuit is critical. It is also closely related to the design of the protection circuit.

High dv/dt can cause unintended turn-on in the opposing-arm IGBT, gate overvoltage, or noise propagation onto the power-supply lines. Examine optimal drive conditions ($+V_{GE}$, $-V_{GE}$, R_G, C_{GE}) to prevent unintended turn-on, gate overvoltage, and unexpected supply-line noise.

If the wiring between the discrete IGBT and the gate-drive circuit is long, the gate voltage at the device terminals can fluctuate transiently, potentially causing overvoltage failure of the IGBT. To prevent gate overvoltage destruction, implement proper gate-wiring design and verify the gate voltage.

For detailed explanations and precautions, refer to Chapter 7, “Gate Drive Circuit Design”

8. Parallel Connections

When applying discrete IGBTs to high current applications, devices are connected in parallel.

When using parallel connections, it is important to design so that each device carries equal current. If current sharing is unequal, one device may be overloaded and fail.

Current balance in parallel operation depends on device characteristics and wiring methods, so it is necessary to manage and design for matching the C–E saturation voltages $V_{CE(sat)}$ of all parallel devices and to keep the main circuit wiring lengths equal.

For detailed explanations and precautions, refer to Chapter 8, “Parallel Connection of Discrete IGBTs.”

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9. Application of TO-247-4

TO-247-4 can reduce loss and suppress ringing by mitigating the effects of inductive voltage (L·dI_C/dt), but this increases the switching speed. In other words, compared with TO-247, dI_C/dt becomes larger, so care must be taken because the surge voltage generated at turn-off is higher. As shown in Fig. 3-4, under the condition I_C = 100 A, with the TO-247 and R_G = 20 Ω, $V_{CE(peak)}$ ≈ 810V. However, to keep the same $V_{CE(peak)}$ with TO-247-4, R_G of approximately 51 Ω must be selected. Also, increasing R_G increases loss, preventing the TO-247-4's low loss feature from being fully realized.

Therefore, for the peripheral circuits of both TO-247 and TO-247-4, select appropriate component values for each device and design the circuit with sufficient margin so that the surge voltage does not exceed the maximum rating.

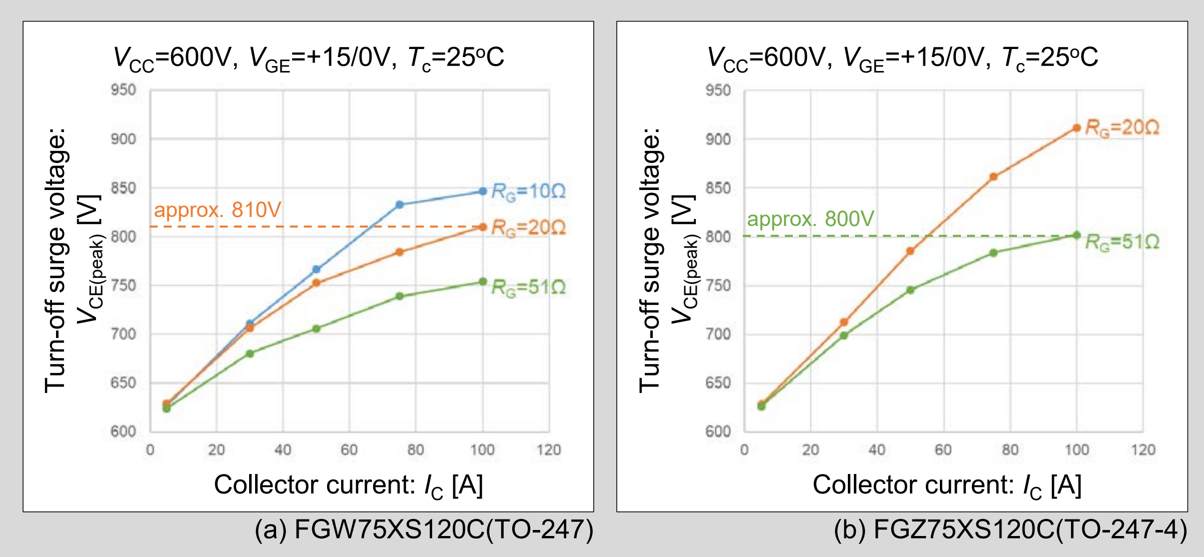

Fig. 3-4 Turn-off surge voltage comparison

By designing a printed circuit board with the layout shown in Fig. 3-5, it is possible to have compatibility between TO-247 and TO-247-4 products. This design makes it easy to replace products and enables two types of packages to be mounted on a single printed circuit board. However, the peripheral circuit constants should be set appropriately for each product.

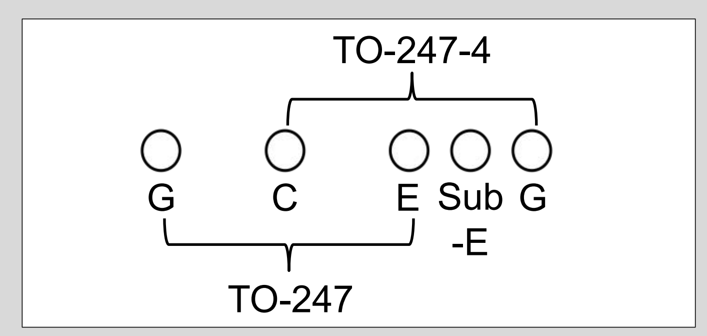

Fig. 3-5 Printed circuit board design example

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10. Mounting Notes

When mounting the discrete IGBT to a heat sink, it is recommended to apply thermal grease thinly and evenly between the device and the heat sink to improve thermal conductivity and enhance heat dissipation. Insufficient amount or improper application of thermal grease may prevent it from spreading over the entire device surface, leading to degraded cooling performance and potential thermal failure.

Depending on the type of thermal grease and the application method used, degradation or depletion of the thermal grease can occur during high temperature operation or under temperature cycling, which may shorten the device lifetime. Please pay close attention to the selection of thermal grease and the method of application.

If the tightening torque of the mounting screws is too low, the thermal resistance will increase, increasing the risk of thermal failure. We recommend using torque values within the range specified in Table 3-2.

Table 3-2 Tightening torque of semiconductor device

Package outline	Mounting hole diameter	Screw	Screw torque (N・cm)
TO-247 TO-247-4	φ3.2	M3	40-60

To fill the gap between the device and the insulating sheet, and between the insulating sheet and the heat sink, apply thermal grease in discrete spots to the case area directly beneath the semiconductor-chip mounting section and to the heat sink surface as shown in Fig. 3-6, then secure to the heat sink with screws tightened with the recommended torque. In addition, the heat sink surface must meet the following conditions.

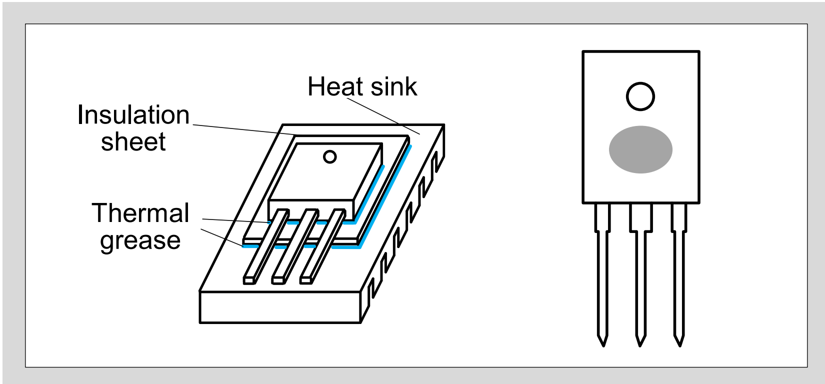

Fig. 3-6 How to apply thermal grease

- Heat sink surface flatness within the contact area of the discrete IGBT: ≤ ±30μm
- Heat sink surface roughness within the contact area of the discrete IGBT: ± 10μm
- Do not taper the screw holes.

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11. Soldering

During soldering, heat (temperature) that exceeds the maximum rated storage temperature will normally be applied to the terminals. Please pay attention to the following precautions when soldering.

Table 3-3 Recommended mounting conditions

Package outline	Mounting method				
	Flow solder (total immersion)	Flow solder (Terminal immersion)	Infrared reflow	Hot air reflow	Soldering iron
TO-247 TO-247-4	Not possible	Possible (within 2 times)	Not possible	Not possible	Possible (only 1 time)

Soldering temperature	Immersion time
260±5°C	10±1 sec
350±10°C	3.5±0.5 sec

- Make sure that the immersion depth of the terminal is at least 1.5mm away from the device body.
- Do not immerse the device body in solder when using flow soldering method.
- If flux is used, avoid chlorine-based types and preferably use rosin-based flux.

12. Cleaning

Please note the following when soldering with flux and subsequently cleaning the flux.

12.1 Solvent

- Use a solvent that is non-flammable, non-toxic, and non-corrosive.
- In particular, avoid trichloroethylene-based solvents, as they contain chlorine.

12.2 Cleaning method

Immersion cleaning is recommended. When performing ultrasonic cleaning, take care that discrete IGBTs or printed circuit boards do not come into direct contact with the vibration source.

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13. Terminal Processing and Mounting

13.1 Stress to the terminals

Discrete IGBT terminals undergo reliability testing in accordance with JEITA standard ED4701/400A, Test Method 401A. Table 3-4 summarizes the individual test items; for full details, please refer to the JEITA specification.

Note that the following tests apply only to unmounted discrete IGBTs. Any discrete IGBTs that have already been solder-mounted or otherwise installed are excluded from the warranty.

Table 3-4 Test items

Test items	Test methods and conditions	Reference item	Number of samples
Tensile test	Tensile force: 2.2 ± 0.1 N Holding time: 30 seconds	JEITA ED4701/400A 401A Method I	15
Bending test	Bending angle: 15 degrees Bending time: 1 time	JEITA ED4701/400A 401A method III	15
Fatigue test	Bending angle: 15 degrees Bending time: 3 times	JEITA ED4701/400A 401A method V	15

13.2 Precautions for terminals forming

When it is unavoidable to form (bend) the terminals to suit component layouts, observe the following.

Use a special jig that does not apply stress to the internal chip and external package.

- Use a dedicated jig that does not apply stress to the internal chip or the external package.
- For lateral (in-plane) bends, bend at a point at least 4.5 mm away from the package, and limit the bend angle to 30° maximum (see Figure 3-7).
- For right-angle bends (out-of-plane) relative to the package, bend at a point at least 4.5 mm from the package.
- Ensure the bend radius (R) is equal to or greater than the terminal thickness.
- Perform forming at any given location only once. Do not reform or attempt to restore the terminal to its original shape.

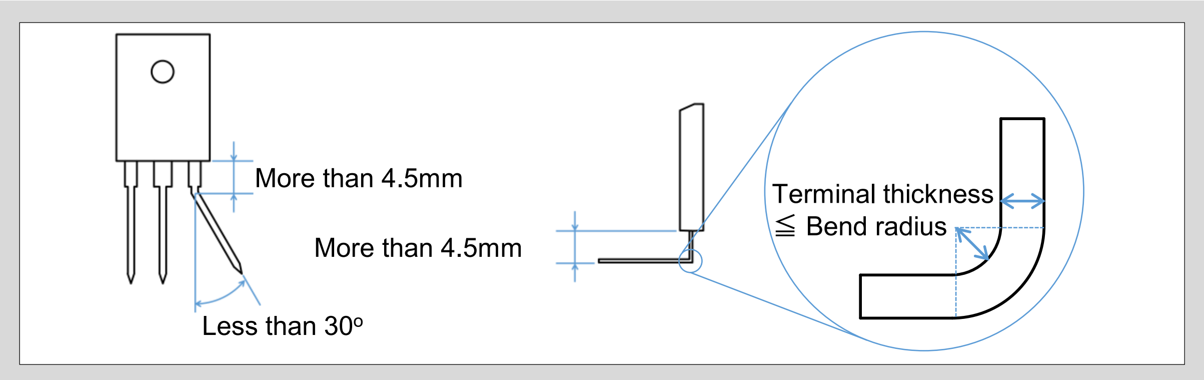

Fig. 3-7 Precautions for terminal forming

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13.3 Insertion into printed circuit board

When inserting into the printed circuit board, ensure that the spacing between the terminals matches the spacing of the printed circuit board holes so as not to impose excessive stress on the terminals.

14. Storage

- Devices should be stored at room temperature and normal humidity—avoid extreme temperatures or humidity. As a guideline, maintain 5–35°C and 45–75% RH. In very dry environments, use a humidifier. Do not use tap water (its chlorine content may cause terminal corrosion); instead use purified water or boiled water.
- Avoid areas where corrosive gases are generated or where there is excessive dust.
- Prevent rapid temperature changes that could cause condensation on the devices; choose a location with stable temperature.
- When stacking outer shipment boxes, limit to five boxes high and take measures to prevent collapse or deformation. Do not place heavy objects on top.
- Store the terminals unprocessed to avoid soldering defects due to rust, etc.
- To avoid solderability defects from rust, keep each terminal in unprocessed state.
- All storage shelves should be made of metal and grounded.
- The storage period is one year from the date of delivery, provided that the above points are observed in the storage and packing conditions.

15. Transportation

- Avoid extreme forces such as dropping or shock when transporting the products.
- When transporting several products in the same box or container, insert padding between the products to protect the terminals and to keep the products from shifting.
- Take measures against static electricity from being applied to the gate terminals, such as using antistatic bag or shorting the gate and emitter with aluminum foil when transporting the product.

Fig. 3-8 Conductive bag

Fig. 3-9 Conductive foam

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16. Precautions for Use

- Do not touch the product terminals or packages directly during operation or while the product is energized. Doing so may result in electric shock or burns.
- Be sure to install fuses, circuit breakers, etc. of appropriate capacity to prevent secondary damage (fire, explosion, etc.) in the event of unexpected device failure.
- The product becomes hot during operation. Although flame-retardant materials are used for the sealing resin of the product, it may cause smoke or fire if the product fails. If the product is used in flammable environment (e.g. environment where flammable gases may leak or accumulate) or near combustible materials, be sure to take fire spread prevention measures at your own responsibility.
- Evaluate the package temperature, junction temperature and terminal temperature rise.
- Do not use the product in environments containing acid, organic matter, or corrosive gas (e.g. hydrogen sulfide, sulfurous acid gas, etc.), as this may cause the product to oxidize or corrode, resulting in failure.
- The product is not designed to be radiation resistant. Avoid using it in environments where it may be exposed to radiation.
- As shown in Fig. 3-10, design and use the device with a steady-state voltage not exceeding 80% of the absolute maximum rated voltage. Even under worst-case conditions, keep the applied voltage within the absolute maximum rated voltage.

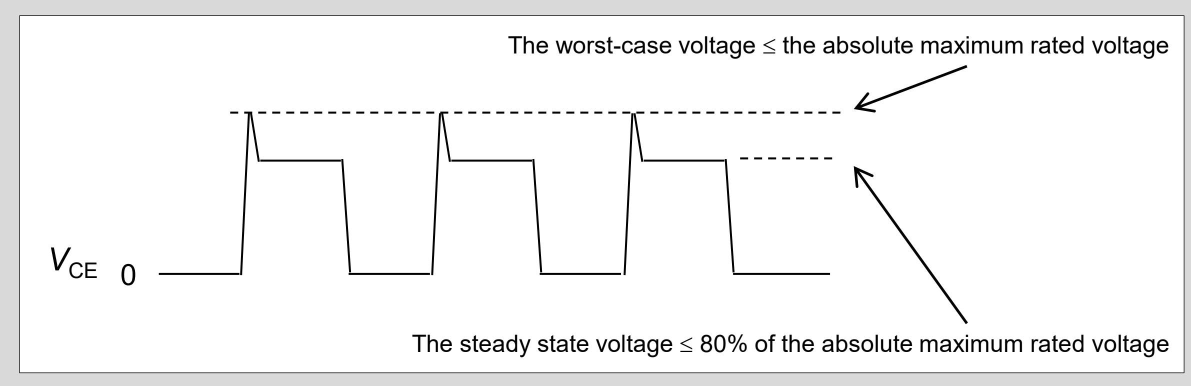

Fig. 3-10 Voltage waveform during switching

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Chapter 4 Typical Troubles and Troubleshooting

1. Troubleshooting	4-2
2. IGBT Test Procedures	4-7
3. Typical Troubles and Troubleshooting	4-9

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This chapter describes typical troubles and how to deal with them.

1. Troubleshooting

Abnormality such as incorrect wiring or mounting of discrete IGBTs in inverter circuit, etc., could cause device destruction. Because there are many failure modes, it is important to first determine the cause of the problem and take the necessary countermeasures. Table 4-1 shows how to determine a device failure modes as well as the causes by observing the device external abnormalities. First of all, check the estimated failure mode from Table 4-1. If the cause cannot be determined using this table, use the detailed analysis charts in Fig. 4-1. In addition, method to determine whether the device is broken is described in section 4.2, and typical troubles and their countermeasures are described in section 4.3. These can be used to assist in finding the cause.

Table 4-1 Estimation of failure modes and causes of elements

External abnormalities		Cause		Failure mode	Checkpoints
Short circuit	Arm short circuit	Surge voltage during short circuit protection exceeds SCSOA.		SCSOA (surge voltage)	Check that short circuit waveform (locus) and device ruggedness match.
	Series arm short circuit	Insufficient dead time	Insufficient $-V_{GE}$ Dead time setting error	Overheating	Check that device t_{off} and dead time match.
		dv/dt malfunction	Insufficient $-V_{GE}$ Gate wiring too long	SCSOA and overheating	Check for false turn-on caused by dv/dt.
		Noise, etc.	Logic or gate drive circuit malfunction		Check for circuit malfunction.
	Output short circuit	Miswiring, abnormal wire contact, or load short circuit.			Check conditions at time of failure. Check that device ruggedness and protection circuit match. Check wiring condition.
	Ground fault	Miswiring, abnormal wire contact			
Overload (overcurrent)		Logic circuit malfunction		Overheating	Check logic circuit.
		Overcurrent protection circuit setting error			Adjust overcurrent protection level.
Overvoltage	Excessive DC voltage	C-E voltage exceeds voltage rating	Excessive input voltage Overvoltage protection setting error	C-E overvoltage	Adjust overvoltage protection level.
	Excessive surge voltage	Surge voltage during turn-off exceeds RBSOA		RBSOA	Check that turn-off waveform (locus) and RBSOA match. Review snubber circuit.
		Surge voltage during FWD reverse recovery exceeds voltage rating		C-E overvoltage	Check that surge voltage and voltage rating match. Review snubber circuit.
		Short on-pulse reverse recovery	Logic or gate drive circuit malfunction due to noise		Check logic circuit.
			Interference to gate signal from the main circuit, etc.		Check gate signal. Use twisted pair wire. Check distance between main circuit and signal wire.
Drive supply voltage drop		V_{GE} drops resulting in increased heat (loss) generation	DC-DC converter malfunction Drive voltage rise is too slow. Disconnected wire	Overheating	Check for circuit malfunction.
Gate overvoltage		Static electricity applied to gate		G-E overvoltage	Check operating conditions (anti-static protection).
		Surge voltage due to excessive length of gate wiring			Check gate voltage.
Driving IGBT with gate open		Applying voltage at C-E with the gate open		Overheating	Check gate voltage.
Overheating	Insufficient heat dissipation	T_{vj} exceeds maximum value	Loose screws Insufficient thermal grease Cooling fan stopped	Overheating	Check cooling conditions.
	Increased loss	Logic circuit malfunction			Check logic circuits.
Stress	Stress	Soldering inside the module disconnected due to stress fatigue	Stress from external wiring	Disconnection of internal circuit (open)	Check the generated stress. Check the mounting condition of the module and other mounting parts.
	Vibration		Stress from vibration of other mounting parts		
Reliability (Lifetime)		The application conditions do not match the reliability of the module		Failure mode is different for each case	Refer to Fig. 4-1.

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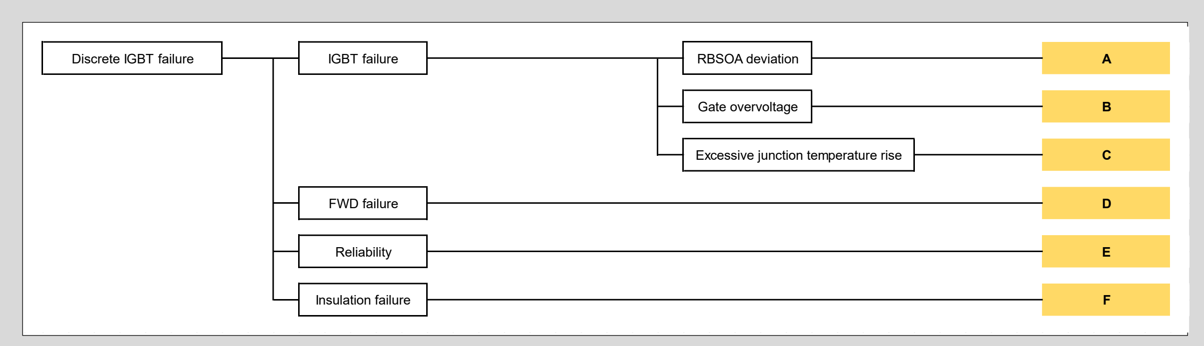

Fig. 4-1(a) Discrete IGBT failure analysis chart (* Symbols A to E are linked to the charts below)

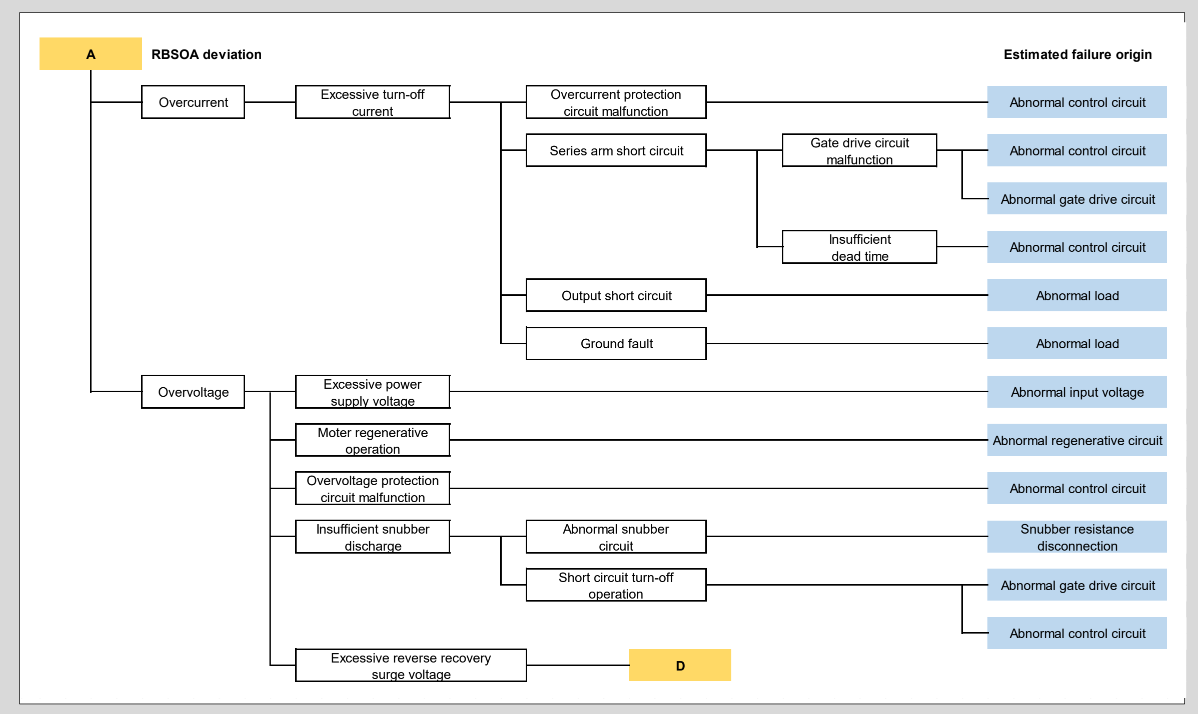

Fig. 4-1(b) Mode A: RBSOA deviation

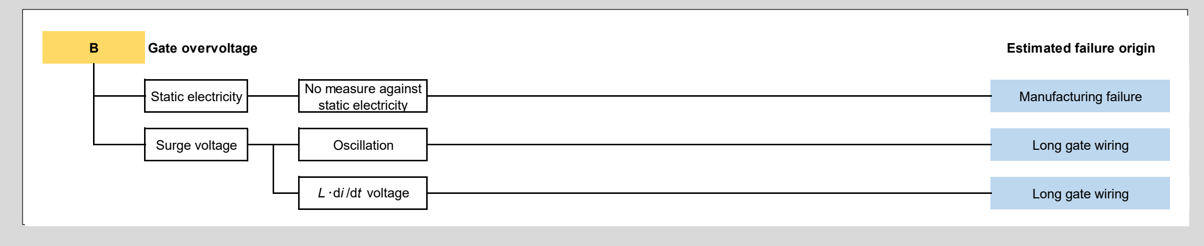

Fig. 4-1(c) Mode B: Gate overvoltage

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C Excessive junction temperature rise — Estimated failure origin

- Conduction loss increase
  - Saturation voltage increase
    - Insufficient forward bias gate voltage → Abnormal gate drive circuit; Abnormal control circuit power supply
  - Collector current increase
    - Overcurrent
      - Overcurrent protection circuit malfunction → Abnormal control circuit
      - Series arm short circuit
        - Gate drive circuit malfunction → Abnormal control circuit; Abnormal gate drive circuit
        - Insufficient dead time → Abnormal control circuit
      - Output short circuit → Abnormal load
      - Ground fault → Abnormal load
    - Overload → Abnormal control circuit; Abnormal load
- Switching loss increase
  - Number of switching increase
    - Carrier frequency increase → Abnormal control circuit
    - di /dt malfunction → Abnormal snubber circuit; Abnormal gate drive circuit
    - Gate drive signal malfunction → Abnormal control circuit; Abnormal gate drive circuit
  - Turn-on loss increase
    - Turn-on time increase
      - Insufficient forward bias gate voltage → Abnormal gate drive circuit
      - Gate resistance increase → Abnormal gate drive circuit
    - Excessive turn-on current
      - Excessive snubber discharge current → Abnormal snubber circuit
      - Series arm short circuit → Insufficient dead time → Abnormal control circuit
  - Turn-off loss increase
    - Turn-off time increase
      - Insufficient reverse bias gate voltage → Abnormal gate drive circuit
      - Gate resistance increase → Abnormal gate drive circuit
    - Series arm short circuit
      - Insufficient dead time → Abnormal control circuit; Abnormal gate drive circuit
- Contact thermal resistance increase
  - Insufficient tightening torque → Insufficient mounting torque
  - Insufficient heat sink flatness → Hat sink warpage
  - Insufficient thermal grease volume → Insufficient thermal grease adjustment
- Case temperature rise
  - Decreased cooling capacity
    - Clogged heat sink → Insufficient dust filtration
    - Cooling fan speed decreased,stopped → Abnormal cooling fan
  - Abnormal ambient temperature rise
    - Partial overheating → Abnormal cooling system
  - Overheating protection malfunction → Abnormal overheating protection system

Fig. 4-1(d) Mode C: Excessive junction temperature rise

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D **FWD failure** — **Estimated failure origin**

- Excessive junction temperature rise
  - Conduction loss increase
    - Overload
      - Power factor drop
      - Abnormal load
      - Abnormal control circuit
  - Switching loss increase
    - Number of switching increase
      - dv/dt malfunction
        - Abnormal snubber circuit
        - Abnormal gate drive circuit
      - Gate drive signal malfunction
        - Abnormal control circuit
        - Abnormal gate drive circuit
      - Carrier frequency increase
        - Abnormal control circuit
  - Contact thermal resistance increase
    - Insufficient tightening torque
      - Insufficient tightening torque
    - Insufficient heat sink flatness
      - Heat sink warpage
    - Insufficient thermal grease volume
      - Insufficient thermal grease adjustment
  - Case temperature rise
    - Decreased cooling capacity
      - Clogged heat sink
        - Insufficient dust filtration
      - Cooling fan speed decreased, stopped
        - Abnormal cooling fan
    - Abnormal ambient temperature rise
      - Partical overheating
        - Abnormal cooling system
    - Overheating protection malfunction
      - Abnormal overheating protection system
- Overvoltage
  - Excessive reverse recovery surge voltage
    - Abnormal snubber circuit
    - Turn on di/dt increase
      - Insufficient forward bias gate voltage
        - Abnormal gate drive voltage
      - Gate resistance decrease
        - Abnormal gate drive circuit
    - Short on-pulse reverse recovery phenomenon
      - Gate signal interruption due to noise, etc.
        - Abnormal gate drive circuit
        - Abnormal control circuit
  - Excessive turn-off surge voltage
    - A
- Overcurrent
  - Large charging current in converter applications
    - Abnorml charging circuit

Fig. 4-1(e) Mode D: FWD failure

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E **Failure due to product handling and reliability** — **Estimated failure origin**

- Failure due to product handling
  - External force, load
    - Loading during product storage → Loading conditions
    - Stress generated in terminals when mounted → Terminal stress
  - Excessive tightening torque → Tightening part
  - Insufficient screw tightening torque
    - Excessive contact thermal resistance → Tightening part
  - Vibration
    - Excessive vibration during transportation → Transportation conditions
    - Loose mounting → Terminal part
  - Impact
    - Drops, collisions, etc. during transportation → Transportation conditions
  - Heat resistance of solder terminals
    - Excessive temperature during soldering → Assembly conditions during product mounting
  - Storage under abnormal conditions
    - Storage in corrosive gas atmosphere → Storage conditions
    - Storage in condensation prone environment → Storage conditions
    - Storage in dusty environment → Storage conditions
  - Destruction during parallel connection
    - Transient current concentration/oscillation caused by poor main circuit wiring uniformity → Uniformity of main circuit wiring
- Failure due to reliability (lifetime)
  - High temperature storage → Storage conditions
  - Low temperature storage → Storage conditions
  - High temperature and humidity storage → Storage conditions
  - Thermal stress failure caused by repetitive gradual rise and fall of product temperature (temperature cycle, ΔT_C power cycle) → Matching between working conditions and product lietime
  - Thermal stress failure caused by sudden rise or fall of product temperature (thermal shock) → Matching between working conditions and product lietime
  - Thermal stress failure of product internal wiring caused by repetitive chip temperature change due to sudden load change, etc. (ΔT_{vj} power cycle) → Matching between working conditions and product lietime
  - Long-term voltage application at high temperature (high temperature bias (between C-E and G-E)) / Long-term application at high temperature → Matching between working conditions and product lietime
  - Long-term voltage application at hot and humid condition (temperature humidity bias (THB)) / Long-term application at hot and humid condition → Matching between working conditions and product lietime

Fig. 4-1(f) Mode E: Failure due to product handling and reliability

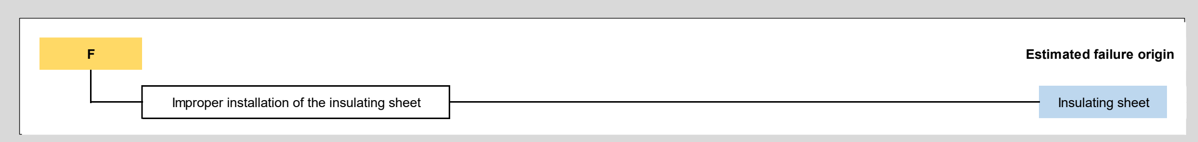

Fig. 4-1(g) Mode F: Improper installation of the insulating sheet

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2. IGBT Test Procedures

An IGBT device that has been found to be faulty can be checked by using a transistor characteristics measuring device called a 'transistor curve tracer (CT)'.

(1) G-E leakage current

(2) C-E leakage current (short G-E)

If a CT is not available, other test equipment such as a tester that is capable of measuring voltage/resistance can be used to help to diagnose the module.

2.1 G-E leakage current check

As shown in Fig.4-2, measure the leakage current or resistance between G-E, with C-E shorted. (Do not apply a voltage in excess of 20V between G-E. If a tester is used, make sure that the internal battery voltage is less than 20V.)

If the module is normal, the leakage current reading will be on the order of several 100nA (if a tester is used, the resistance reading will be on the order of 10MΩ to infinity). Otherwise, the device has most likely destroyed (generally, if a device is destroyed, G-E will be short-circuited).

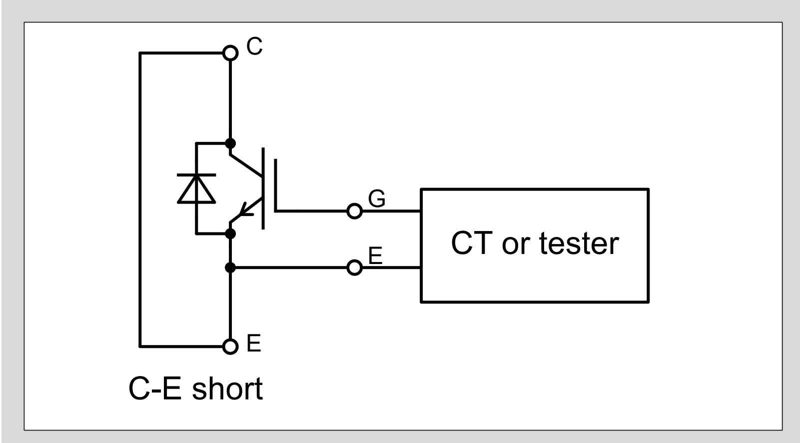

Fig. 4-2 G-E check

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2.2 C-E leakage current check

As shown in Fig.4-3, measure the leakage current or resistance between C-E, with G-E shorted. Be sure to connect C to (+) and E to (-). If the polarity is reversed, the FWD will conduct and shorts C-E.

If the module is normal, the leakage current reading should read below the I_{CES} maximum value specified in the datasheet (if a tester is used, the resistance reading will be on the order of 10MΩ to infinity). Otherwise, the device has most likely destroyed (generally, if a device is destroyed, C-E will be short-circuited).

Caution: Never perform withstand voltage measurement between C-G. It might cause the dielectric breakdown of the oxide layer due to excessive voltage.

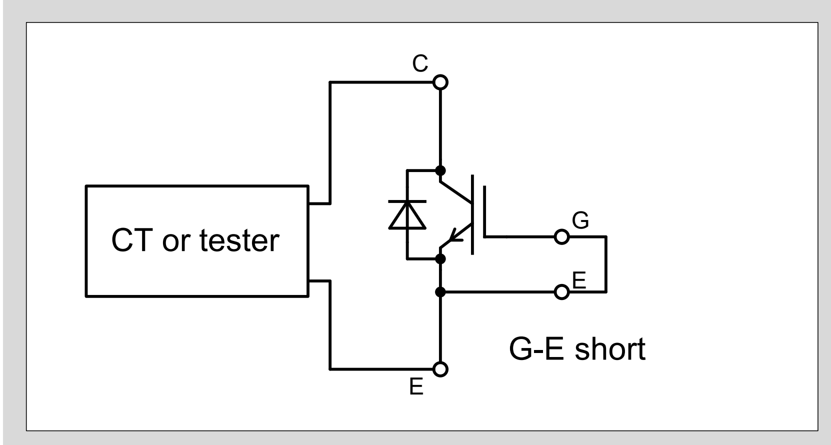

Fig. 4-3 C-E check

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3. Typical Troubles and Troubleshooting

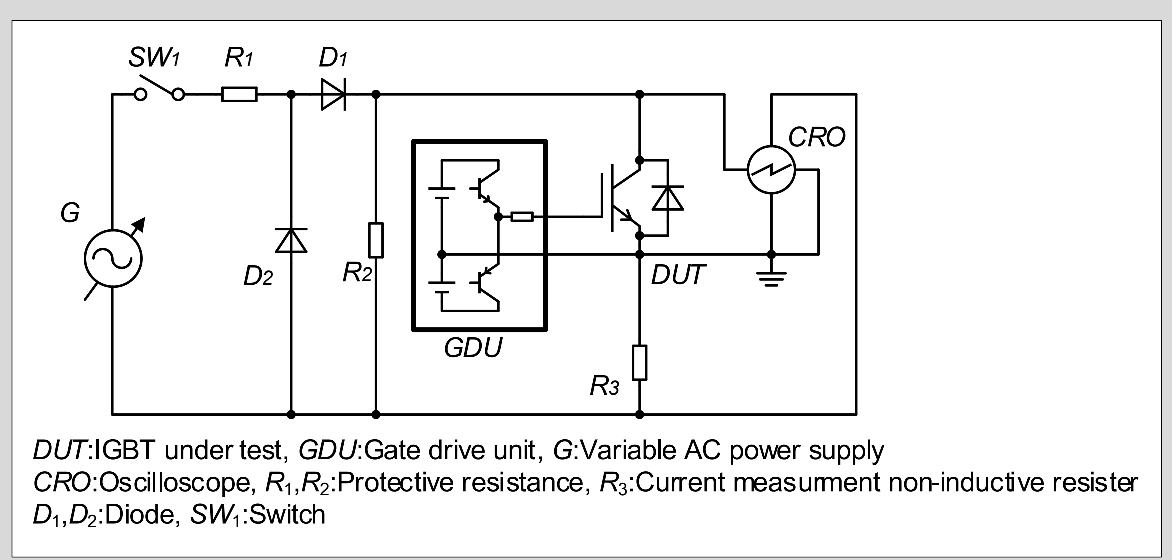
3.1 Main circuit voltage application with G-E open

If main circuit voltage is applied with G-E open, the IGBT would be turned on autonomously, triggering a large current flow and cause device destruction. This phenomenon occurs when the G-E capacitance is charged through the feedback capacitance C_{res} of the IGBT, raising the gate potential and causing the IGBT to be turned on. Take measures such as connecting a resistor of about 10kΩ to G-E to prevent G-E from being opened (refer to Chapter 3, section 2).

If the gate signal line is switched using a mechanical switch, such as a rotary switch during product acceptance testing or on similar occasions, the G-E may open instantaneously at the time of switching, which could cause device destruction if voltage is applied to C-E.

When the mechanical switch chatters, a similar period is generated, leading to device destruction. To prevent this, be sure to discharge the main circuit voltage to 0V before switching the gate signal. Furthermore, when conducting characteristics test, such as acceptance test on a product comprising multiple devices (two or more), be sure to short G-E of the devices other than the one under test.

Fig. 4-4 shows an example of an on-voltage measurement circuit. The measurement procedure is described using this circuit. First, turn off the gate drive unit (GDU) ($V_{GE} \leqq$ 0V), then turn on SW_1 to apply voltage to C-E. Next, apply a predefined forward bias voltage to G-E from the GDU to turn-on the IGBT and measure the on voltage. Finally, turn off the gate circuit and then turn off SW_1. This sequence allows for safe measurement of device characteristics without risking destruction.



DUT:IGBT under test, *GDU*:Gate drive unit, *G*:Variable AC power supply
CRO:Oscilloscope, R_1,R_2:Protective resistance, R_3:Current measurment non-inductive resister
D_1,D_2:Diode, SW_1:Switch

Fig. 4-4 On voltage measurement circuit

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3.2 False turn-on of the IGBT caused by insufficient -V_{GE}

Insufficient reverse bias gate voltage -V_{GE} induces false turn-on of the IGBT, resulting in short circuit of both the upper and lower arm IGBTs. The product may be destroyed by the surge voltage or loss generated when the short circuit current is cut off. Therefore, make sure that false turn-on does not happen when designing the equipment (recommended -V_{GE}=15V). In addition, please refer to Chapter 7, section 1.4 for the details of the malfunction occurrence mechanism due to the d*v*/d*t* when -V_{GE} is insufficient.

Fig. 4-5 shows an example of how to check the presence of short circuit current in the upper and lower arms. First, disconnect the output terminals (U, V, W) of the inverter (open, no load). Next, start the inverter and drive each IGBT. At this time, if the current flowing from the power supply line is detected as shown in the figure., the presence of short circuit current can be checked. If -V_{GE} is sufficient, only a very small pulse current (about 5% of the rated current) that charges the junction capacitance of the device will be observed. However, if -V_{GE} is insufficient and short circuit occurs, this current will increase. To make an accurate judgment, it is recommended to perform this current measurement with -V_{GE}=15V first, and then measure the current again with the specified -V_{GE}. If the current of both cases have the same value, it means that there is no false turn-on.

If false turn-on is confirmed by the above method, countermeasures include increasing -V_{GE} until the short circuit current disappears, or connect a capacitor (C_{GE}) with capacitance of about twice the value of C_{ies} described in the specifications between G-E. Is recommended to connect C_{GE} close to the gate terminals.

However, simply adding C_{GE} will increase the switching time and loss. In order to have equivalent switching time and loss before C_{GE} addition, it is recommended to decrease the R_G value to about half of that before C_{GE} addition.

Another cause of short circuit through the upper and lower arms is insufficient dead time. When this happens, short circuit current will be observed in the test. If the short circuit current does not decrease even when -V_{GE} is increased, increasing the dead time is necessary. Please refer to Chapter 7, section 3 for a detailed explanation of dead time.

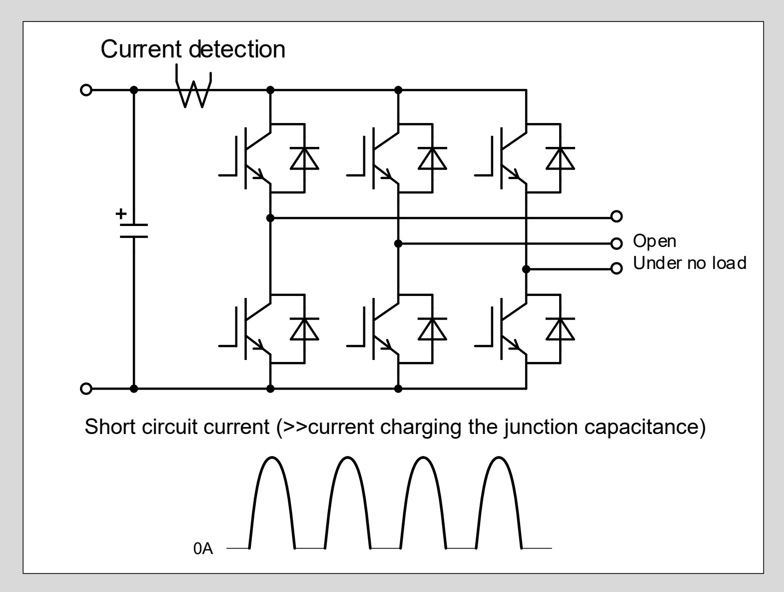

Fig. 4-5 Short circuit current measuring circuit

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3.3 Diode reverse recovery from a transient on state (short on-pulse reverse recovery)

Some discrete IGBT contains built-in FWD. Paying close attention to the behavior of this FWD is very important for designing a reliable equipment. This section describes the short on-pulse reverse recovery phenomenon, which is likely to lead to device failure.

The short on-pulse reverse recovery phenomenon is a phenomenon in which the gate signal is interrupted due to noise, etc. when driving the IGBT, resulting in a very large reverse recovery surge voltage. Fig. 4-6 shows the waveforms of short on-pulse reverse recovery. If a very short off-pulse (T_w) with respect to the on period (T_{ON}) of IGBT is generated, the FWD on the opposite arm will enter reverse recovery in a very short time after it is turned on. Normally, reverse recovery starts after sufficient carriers are accumulated in the FWD, whereas in the short on-pulse reverse recovery, reverse recovery starts without sufficient carrier accumulation in the FWD. As a result, the depletion layer of FWD expands at a rapid speed, causing steep d*i*/d*t* and d*v*/d*t*. This causes a very large reverse recovery surge voltage to occur between C-E (K-A). If the surge voltage exceeds the device rated voltage, it may lead to device failure.

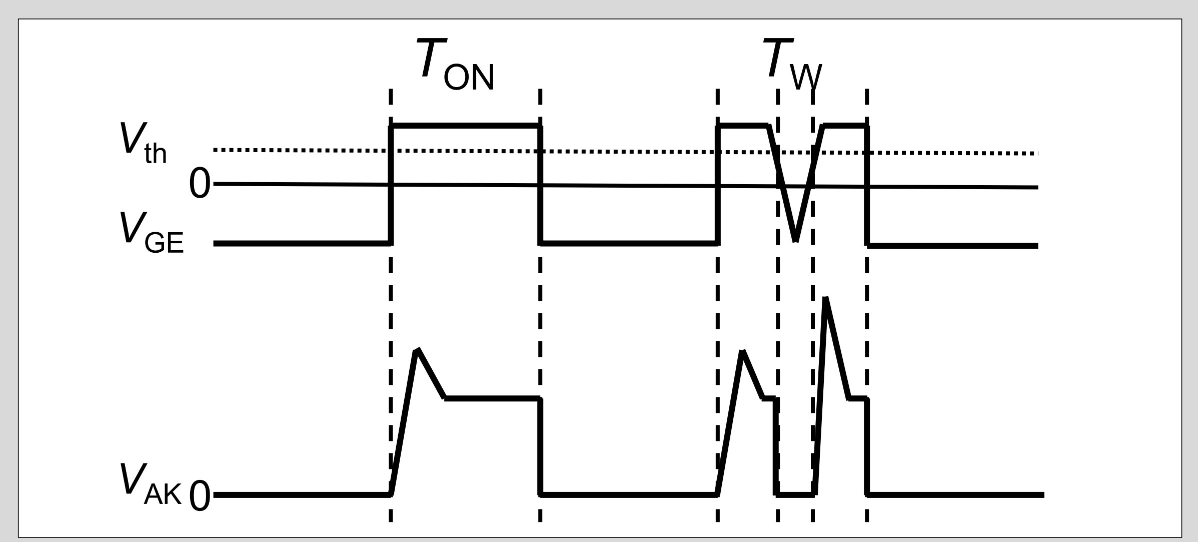

Fig. 4-6 Waveforms of short on-pulse reverse recovery

When designing your equipment, verify that the surge voltage at minimum T_w does not exceed the device rated voltage. If the surge voltage exceeds the device rated voltage, implement one or more of the following countermeasures.

- Increase R_G
- Reduce circuit inductance
- Enhance snubber circuit
- Add C_{GE}
- Add active clamping circuit

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3.4 EMC noise countermeasures

Power converters often need to comply with Europe's CE-marking requirements or Japan's VCCI standards. Suppressing EMI noise, both conducted and radiated below the regulatory limits is therefore a critical design task.

Discrete IGBTs have been pushed toward ever faster switching and lower loss. As a result, the high d*v*/d*t* and d*i*/d*t* generated when switching IGBTs increasingly become a source of radiated noise. In particular, the steep transitions at turn-on, when the FWD in the opposite arm undergoes reverse recovery, can excite high-frequency LC resonances between the semiconductor's junction capacitances and the wiring inductances, leading to significant radiated emissions.

To reduce radiated noise from discrete IGBTs, it is effective to "soften" the switching waveforms, especially the turn-on edge, by revising the gate drive conditions. Refer to Chapter 7 for guidelines on selecting appropriate gate drive parameters. Note, however, that slowing the switching transitions will tend to increase switching loss. Therefore, it is important to balance noise reduction against efficiency, taking into account the converter's operating conditions and the IGBT's cooling conditions.

Table 4-2 lists the common measures for reducing radiated noise. Because the actual noise sources and levels depend heavily on each system's wiring layout, materials, and circuit topology, you should validate the effectiveness of these countermeasures in your own design.

Table 4-2 Countermeasures of radiation noise

Countermeasure	Description	Remarks
Review gate drive conditions (reduce d*v*/d*t* and d*i*/d*t*)	Increase the R_G (particularly, turn-on side).	Switching time and switching loss increase.
	Connect a capacitor between G-E (C_{GE}).	Switching time and switching loss increase.
Connect the snubber capacitor as near as possible to the discrete IGBT	Minimize the wiring between the snubber capacitor and the discrete IGBT.	Effective in suppressing surge voltage and d*v*/d*t* during switching.
Reduce wiring inductances	Use laminated bus bars to reduce inductances.	Effective in suppressing surge voltage and d*v*/d*t* during switching.
Filtering	Connect noise filters to the input and output of the equipment.	Various filters are commercially available
Cable shielding	Shield the input/output cables to reduce radiation noise from the cables.	
Metalize the equipment case	Metalize the equipment housing to suppress noise emitted from the device	

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Chapter 5 Protection Circuit Design

1. Short Circuit (Overcurrent) Protection 5-2

2. Overvoltage Protection 5-8

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This chapter describes about the protection circuit design.

1. Short Circuit (Overcurrent) Protection

1.1 Short circuit withstand capability

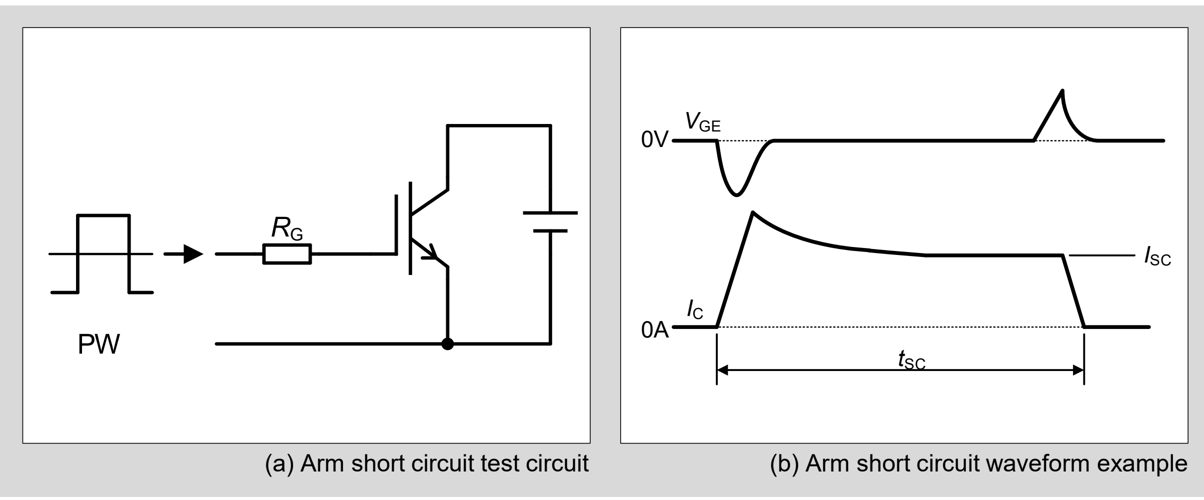
If the equipment experiences a short circuit due to an abnormal condition, the IGBT's collector current I_C rises, and once it exceeds a certain threshold, the C-E voltage V_{CE} abruptly increases. This characteristic limits I_C during a short circuit to below a certain level, but subjects the IGBT to high voltage and large current. If this state persists, the IGBT will be destroyed. The duration that an IGBT can survive such a condition without damage is specified as short circuit withstand capability.

The discrete IGBT XS series is optimized for low switching loss and low saturation voltage, traits that trade off against short circuit withstand capability. Consequently, short circuit withstand capability is not guaranteed for this series. Do not use XS series devices in circuits where short circuit is anticipated.

The concept of short-circuit withstand capability for arm short circuit and output short circuit is explained below.

1.1.1 Arm short circuit

Fig. 5-1 shows an arm short circuit test circuit and waveform example. As for the arm short circuit, the I_C rises sharply at the start of the short circuit and drops slightly after saturation. The short circuit (saturation) current value I_{SC} is determined by V_{GE}, device output characteristics, and T_{vj}, and is almost independent of V_{DC}, R_G, and PW.



(a) Arm short circuit test circuit (b) Arm short circuit waveform example

Fig. 5-1 Arm short circuit test circuit and waveform

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1.1.2 Output short circuit

Fig. 5-2 shows the output short circuit test circuit and waveform example. In the output short circuit, the short circuit wire has inductance component, thus the current waveform at the start of the short circuit is different from that in the case of the arm short circuit. In this case, the current rise rate d*i*/d*t* can be expressed as follows.

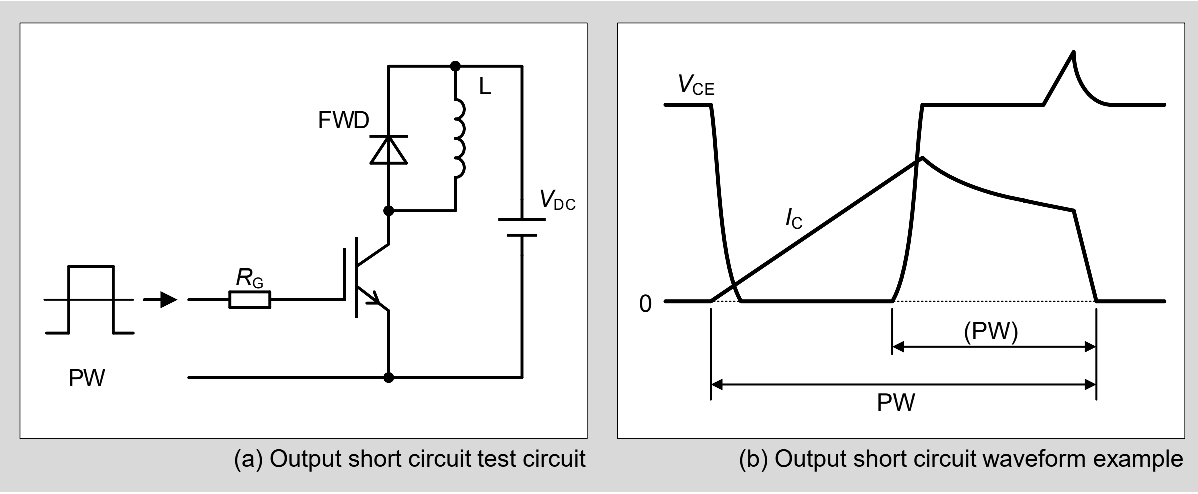
$$d_i/d_t = V_{DC}/L \ \ (A/sec)$$

If the time from the start of the short circuit is given as *t* (sec), I_C can be expressed as follows.

$$I_C = d_i/d_t \cdot t \ (A)$$

The I_C peak value depends on the inductance and the drive circuit (transient V_{GE} rise). After reaching the peak value and saturating, V_{CE} rises sharply. From here, it becomes the same situation with an arm short circuit.

The short circuit withstand capability in the case of output short circuit is shown in Fig. 5-2(b) as (PW). During I_C rise, V_{DC} is applied to the inductance L, and the voltage across the IGBT is about $V_{CE\ (sat)}$, thus the load on the IGBT is extremely low compared to the arm short circuit. Therefore, this period is not included in the short circuit withstand capability.



(a) Output short circuit test circuit

(b) Output short circuit waveform example

Fig. 5-2 Output short circuit test circuit and waveform

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1.2 Short circuit modes and causes

Table 5-1 shows the short circuit modes and causes that occur in inverters.

Table 5-1 Short circuit modes and causes

Short circuit mode	Cause
Arm short circuit	IGBT or diode destruction.
Series arm short circuit	Control circuit / drive circuit failure or malfunction due to noise.
Output short circuit	Miswiring or dielectric breakdown of load
Ground fault	Miswiring or dielectric breakdown of load

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1.3 Short-Circuit Detection Methods

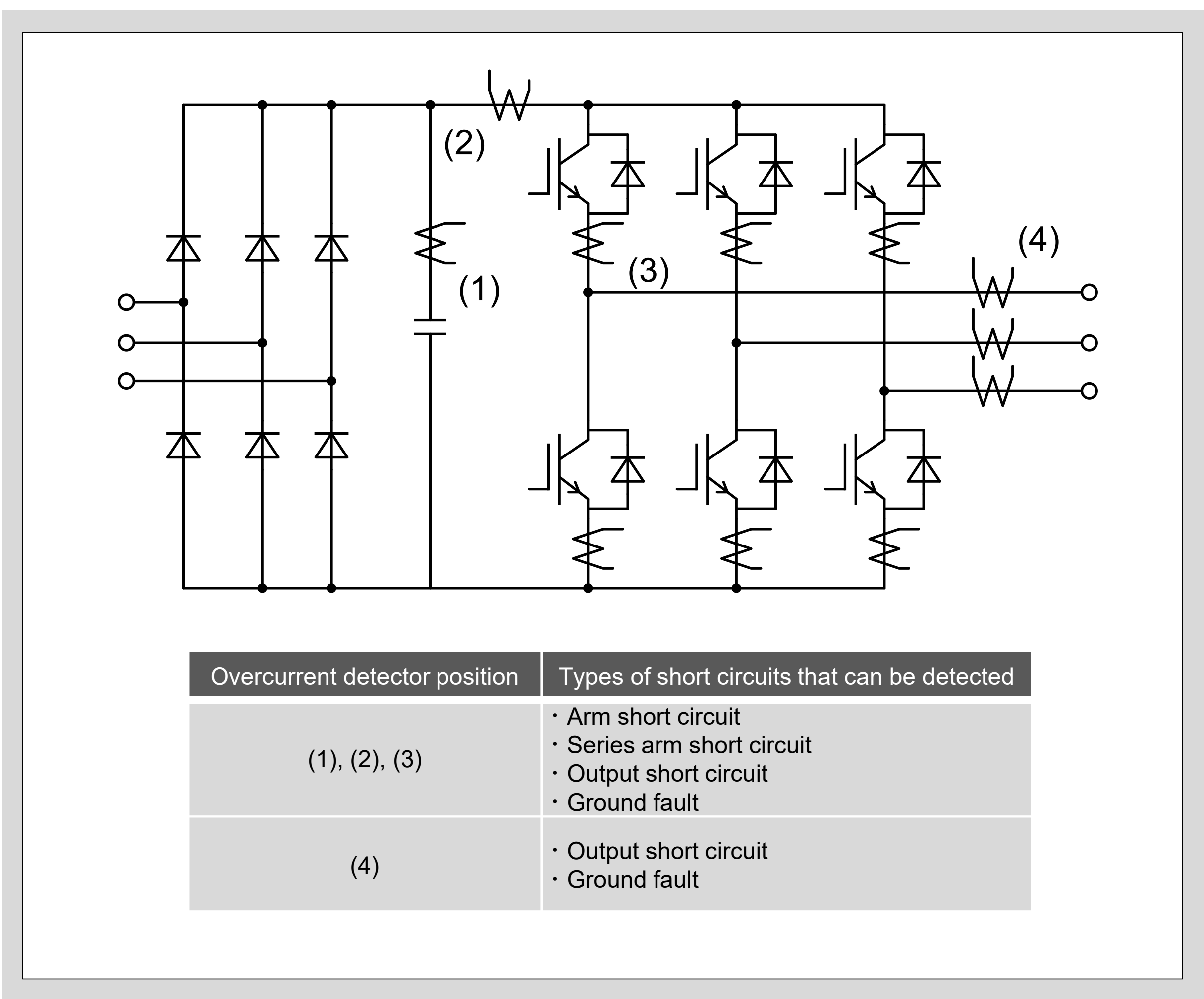
The following describes methods for detecting a short circuit. Note that these techniques are only valid for the V-series IGBTs. Do not use the XS-series in circuits where a short circuit may occur.

1.3.1 Detection by overcurrent detector

As mentioned, in the event of a short circuit, the IGBT must be turned off as soon as possible. Therefore, the time from short circuit detection to the completion of turn-off must be as short as possible.

Since the IGBT turns off very fast, if the short circuit is turned off with a normal gate drive signal, a large surge voltage will be generated, and the IGBT may be destroyed by overvoltage (RBSOA destruction). Therefore, it is recommended to turn off the IGBT slowly (soft turn-off).

Fig. 5-3 shows the overcurrent detectors position in an inverter circuit, and Table 5-2 shows the features and the types of short circuit that can be detected by each method. Consider what kind of protection is necessary and select the most appropriate form of detection.



Overcurrent detector position	Types of short circuits that can be detected
(1), (2), (3)	・Arm short circuit ・Series arm short circuit ・Output short circuit ・Ground fault
(4)	・Output short circuit ・Ground fault

Fig. 5-3 Overcurrent detector position

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Table 5-2 Overcurrent detector positions and their features

Overcurrent detector position	Feature	Types of short circuits that can be detected
In series with smoothing capacitor Fig. 5-3/(1)	• AC current transducer can be used • Low detection precision	• Arm short circuit • Series arm short circuit • Output short circuit • Ground fault
At inverter input Fig. 5-3/(2)	• DC current transducer is required • Low detection precision	• Arm short circuit • Series arm short circuit • Output short circuit • Ground fault
In series with each IGBT Fig. 5-3/(3)	• DC current transducer is required • High detection precision	• Arm short circuit • Series arm short circuit • Output short circuit • Ground fault
At inverter output Fig. 5-3/(4)	• AC current transducer can be used for equipment with high frequency output • High detection precision	• Output short circuit • Ground fault

1.3.2 Detection by $V_{CE(sat)}$

This method can protect against all types of short circuit shown in Table 5-1. Since the operations from overcurrent detection to protection are done on the drive circuit side, this method offers the fastest protection possible. Fig. 5-4 shows an example of short circuit protection circuit using $V_{CE(sat)}$ detection method.

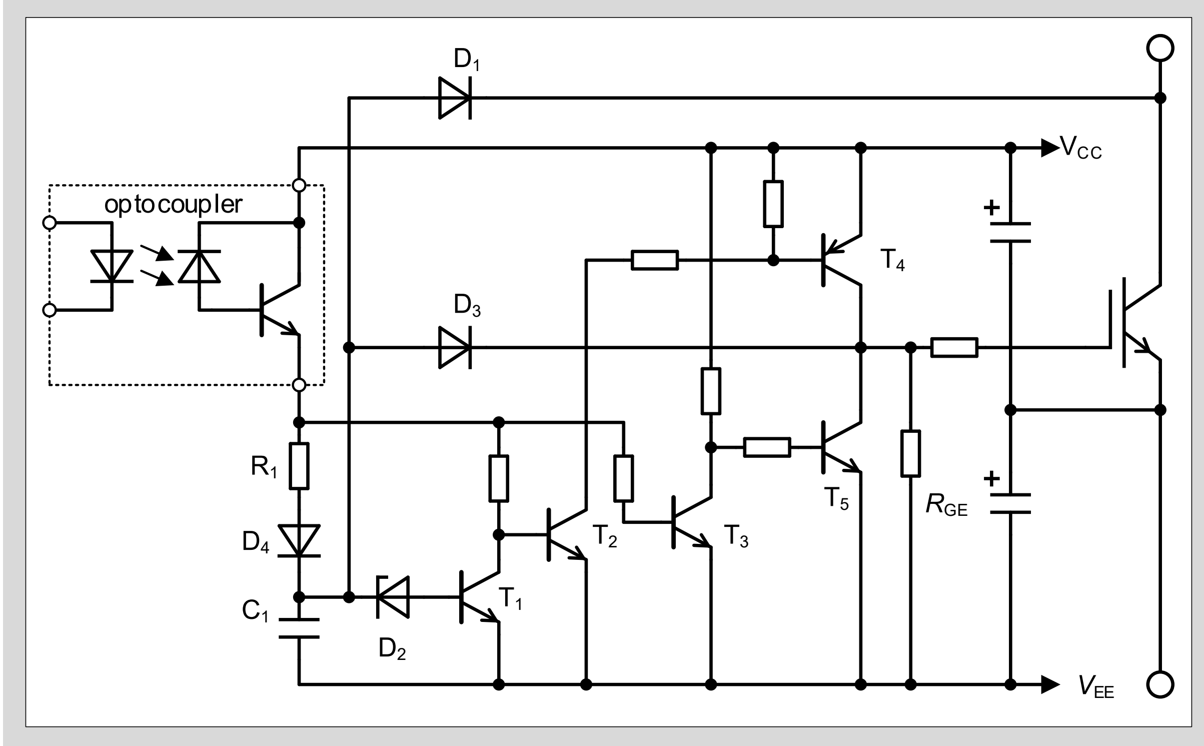

Fig. 5-4 Short-circuit protection circuit using $V_{CE(sat)}$ detection method

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This circuit uses diode D_1 to constantly monitor the C-E voltage.

When the optocoupler is turned on, transistors T_2 and T_4 are turned on and a positive gate voltage is applied to the IGBT. Also, the capacitor C_1 is charged through the resistor R_1 and diode D_4. The operation changes depending on the voltage of capacitor C_1.

【Short circuit protection operation】

If a short circuit occurs after the IGBT is turned on, the V_{CE} of the IGBT rises. When V_{CE} becomes higher than the voltage of [C_1 - D_1 (V_F - V_{EE})], diode D_1 is turned off and the voltage of capacitor C_1 rises again. When the voltage of capacitor C_1 becomes higher than [V_Z of Zener diode D_2 + V_{BE} of transistor T_1], short circuit protection operates.

In the short circuit protection operation, a current flows through Zener diode D_2 to the base of transistor T_1, turning it on. When transistor T_1 is turned on, transistors T_2 and T_4 are turned off, and the applied positive gate voltage is cut off. Since the optocoupler is on, the transistor T_3 is on and transistor T_5 is off. Since the transistors T_4 and T_5 are turned off at the same time, the gate accumulated charge is slowly discharged through the R_{GE}. This effect can suppress the generation of excessive surge voltage when the IGBT turns off. Fig. 5-5 shows an example of the short circuit protection waveform.

【Normal operation】

After the IGBT is turned on, the IGBT is kept on by keeping the voltage of capacitor C_1 below [V_Z of the Zener diode D_2 + V_{BE} of transistor T_1]. When the optocoupler is turned off, the transistors T_2, T_4 turn off, transistor T_3 turns off, and transistor T_5 turns on, applying a negative gate voltage to the IGBT. The charge on capacitor C_1 is discharged through diode D_3 and transistor T_5 and reset to 0V. As can be seen from the above operation sequence, short circuit protection is monitored on each pulse.

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2. Overvoltage Protection

2.1 Cause of overvoltage and suppression methods

2.1.1 Cause of overvoltage

Due to the high switching speed of IGBTs, during turn-off or FWD reverse recovery, the current change rate d*i*/d*t* is very high. Therefore, the circuit wiring inductance around the module L_S can generate a high surge voltage $V_{CEP}=L_S \cdot (di/dt)$.

Fig. 5-5 shows a chopper circuit for measuring the turn-off surge voltage, and Fig. 5-6 shows the switching waveforms.

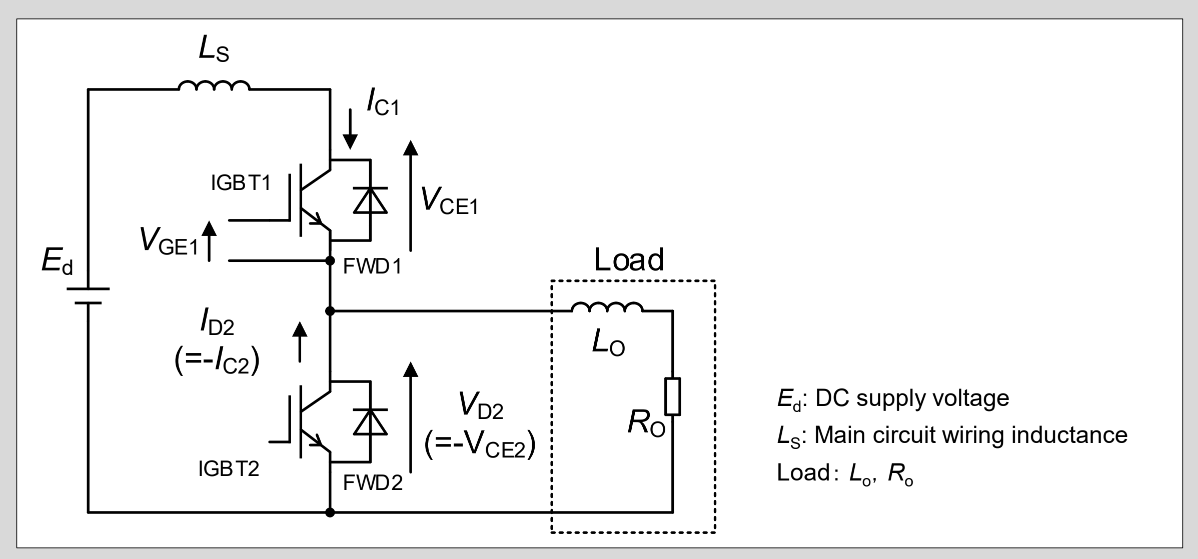

Fig. 5-6 Chopper circuit

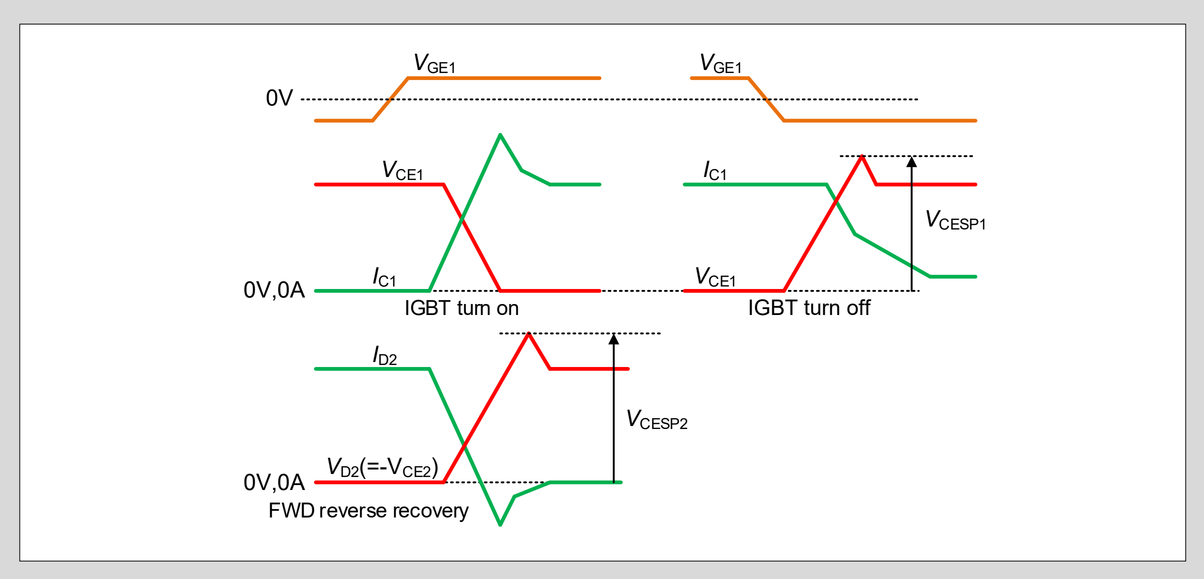

Fig. 5-7 Switching waveforms

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Surge voltage is generated when the IGBT turns off: the rapid change in main-circuit current induces a high voltage across the stray inductance L_s of the main circuit.

The peak value of turn-off surge voltage V_{CESP} can be calculated as follows.

$$V_{\mathrm{CESP}} = V_{\mathrm{CC}} + (-L_{\mathrm{S}} \cdot \frac{dI_C}{dt})$$

dI_C/dt: Maximum I_C change rate at turn-off

If V_{CESP} exceeds the V_{CES} rating, the IGBT will be destroyed.

2.1.2 Overvoltage suppression methods

The following methods are available for suppressing turn-off surge voltage.

- Suppress the surge voltage by adding a protection circuit such as a snubber circuit to the IGBT. Use a film capacitor and place it as close as possible to the IGBT in order to suppress high frequency surge voltage.
- Adjust the $-V_{GE}$ and R_G of the drive circuit in order to reduce the di/dt. (For details, refer to Chapter 7, ‘Gate Drive Circuit Design’)
- Place the DC capacitor as close as possible to the IGBT in order to reduce L_S. Use a low impedance type capacitor.
- Reduce the L_S of the main circuit and snubber circuit by using thicker and shorter wires. It is also very effective to use laminated bus bars.
- Use an active clamp circuit. The surge voltage is suppressed to approximately equal to the Zener voltage of the Zener diode.

2.2 Types of snubber circuits and their features

Snubber circuits can be classified into two types: individual snubber circuit and lump snubber circuit. Individual snubber circuits are connected to each IGBT, while lump snubber circuits are connected between the DC power supply bus and the ground for centralized protection.

2.2.1 Individual snubber circuits

Examples of typical individual snubber circuits are as follows.

- RC snubber circuit
- Charge-discharge RCD snubber circuit
- Discharge-suppressing RCD snubber circuit

Table 5-3 shows the schematic and features of each type of individual snubber circuit.

2.2.2 Lump snubber circuits

Examples of typical lump snubber circuits are as follows.

- C snubber circuit
- RCD snubber circuit

Lump snubber circuits are becoming increasingly popular due to circuit simplification.

Table 5-4 shows the schematic and features of each type of lump snubber circuit.

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Table 5-3 Individual snubber circuits

Snubber circuit schematic	Features (Notes)
RC snubber circuit P N	• The surge voltage suppression effect is greater than that of a lump snubber circuit. • When applied to large capacity IGBTs, the snubber resistance must be low. As a result, the current at turn-on increases and increase the IGBT load.
Charge-discharge RCD snubber circuit P N	• Unlike the RC snubber circuit, a snubber diode is added. Thus, snubber resistance can be increased, and decrease the IGBT load at turn-on . • The power dissipation loss by the snubber resistance of this circuit can be calculated as follows. $P = \frac{L_S \cdot I_O^2 \cdot f}{2} + \frac{C_S \cdot E_d^2 \cdot f}{2}$ L_S: Wiring inductance of main circuit I_O: Collector current at IGBT turn-off C_S: Capacitance of snubber capacitor E_d: DC power supply voltage f: Switching frequency
Discharge-suppressing RCD snubber circuit P N	• Power dissipation loss of snubber circuit is small. • The power dissipation loss by the snubber resistance of this circuit can be calculated as follows. $P = \frac{L_S \cdot I_O^2 \cdot f}{2}$ L_S: Wiring inductance of main circuit Io: Collector current at IGBT turn-off f :Switching frequency

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Table 5-4 Lump snubber circuits

Snubber circuit schematic	Features (Notes)
C snubber circuit	• This is the simplest snubber circuit. • The LC resonance circuit, which consists of main circuit inductance and snubber capacitor, may cause the C-E voltage to oscillate.
RCD snubber circuit	• If the snubber diode is selected incorrectly, a high surge voltage will be generated or the voltage may oscillate during reverse recovery of the snubber diode.

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2.3 Discharge-suppressing RCD snubber circuit design

The discharge-suppressing RCD snubber circuit is considered the most suitable snubber circuit for IGBT. The basic design method of this circuit is as follows.

2.3.1 Study of applicability

Fig. 5-7 shows the turn-off locus of IGBT with discharge-suppressing RCD snubber circuit.

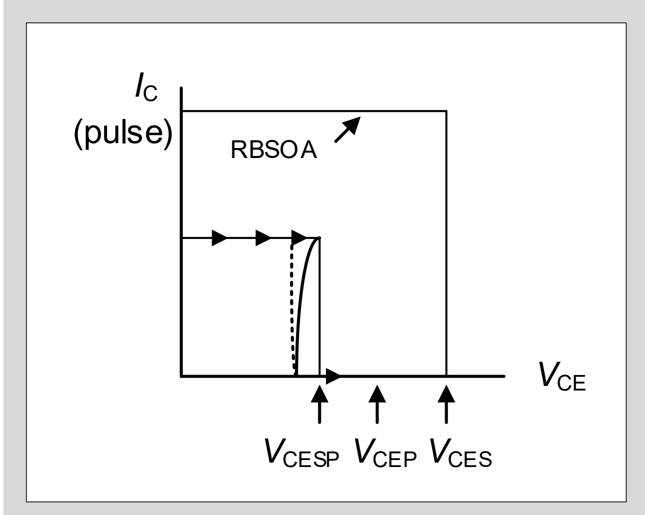

Fig. 5-7 Turn-off locus of IGBT

Fig. 5-8 shows the IGBT turn-off waveform. The discharge-suppressing RCD snubber circuit operates after V_{CE} of the IGBT exceeds the DC power supply voltage. The ideal operation trajectory is shown by the dotted line.

However, in actual equipment, there is surge voltage at turn-off due to the wiring inductance of the snubber circuit and the transient forward voltage of the snubber diode, thus the actual waveform is as shown by the solid line.

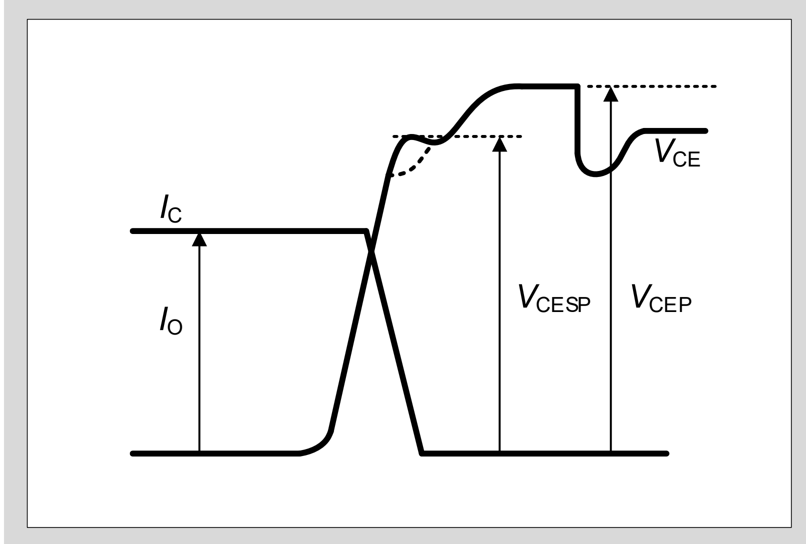

Fig. 5-8 IGBT turn-off waveform

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The discharge-suppressing RCD snubber circuits applicability is decided by whether the turn-off locus after applying the snubber circuit is within the RBSOA.

The surge voltage at IGBT turn-off is calculated as follows.

$$V_{\mathrm{CESP}} = E_{\mathrm{d}} + V_{\mathrm{FM}} + (-L_{\mathrm{S}} \cdot \frac{dI_{\mathrm{c}}}{dt})$$

E_{d} :DC power supply voltage
V_{FM} :Transient forward voltage of snubber diode
The reference values are as follows.
600V class: 20 to 30V
1200V class: 40 to 60V
L :Snubber circuit wiring inductance
dI_c/d_t :Maximum I_{C} change rate at IGBT turn-off

2.3.2 Calculating the snubber capacitance (C_{S})

The capacitance of the snubber capacitor is calculated as follows.

$$C_{\mathrm{S}} = \frac{L_{\mathrm{S}} \cdot I_{\mathrm{O}}^2}{(V_{\mathrm{CEP}} - E_{\mathrm{d}})^2}$$

L_S :Main circuit wiring inductance
I_o :Collector current at IGBT turn-off
V_{CEP} :Snubber capacitor peak voltage
E_{d} :DC power supply voltage

V_{CEP} must be limited to less than V_{CES} of the IGBT. Use a snubber capacitor with good high-frequency characteristics such as a film capacitor.

2.3.3 Calculating the snubber resistance (R_{S})

The function of the snubber resistor is to discharge the accumulated charge in the snubber capacitor before the next IGBT turn-off. To discharge 90% of the accumulated charge by the next IGBT turn-off, the snubber resistance is calculated as follows.

$$R_{\mathrm{S}} \leq \frac{1}{2.3 \cdot C_{\mathrm{S}} \cdot f}$$

R_{S} :Snubber resistance
C_{S} :Snubber capacitance
f :Switching frequency

If the snubber resistance is set too low, the snubber circuit current will oscillate and the peak collector current at the IGBT turn-off will increase. Therefore, set the snubber resistance as high as possible within the calculated range.

Irrespective of the resistance value, the power dissipation of the snubber resistor $P(R_{\mathrm{S}})$ is calculated as follows.

$$P(R_{\mathrm{S}}) = \frac{L_{\mathrm{S}} \cdot I_{\mathrm{O}}^2 \cdot f}{2}$$

$P(R_{\mathrm{S}})$:Power dissipation of snubber resistor
L_{S} :Main circuit wiring inductance
I_o :Collcetor current at IGBT turn-off
f :Switching frequency

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2.3.4 Snubber diode selection

The transient forward voltage of the snubber diode is one of the cause of surge voltage at IGBT turn-off. If the reverse recovery time of the snubber diode is too long, the power dissipation loss of the snubber diode will also be much higher during high frequency switching. Also, if the reverse recovery of the snubber diode is too hard, then the IGBT C-E voltage will oscillate greatly.

Therefore, select a snubber diode that has a low transient forward voltage, a short reverse recovery time, and a soft reverse recovery.

2.3.5 Snubber circuit wiring precautions

The snubber circuit wiring inductance is one of the main cause of surge voltage, therefore it is important to reduce the wiring inductance, as well as considering the layout of circuit components.

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2.4 Overvoltage suppression circuit -example of clamp circuit configuration-

In general, surge voltage can be suppressed by means of decreasing the stray inductance or installing a snubber circuit. However, it may be difficult to suppress the surge voltage under depending on the operating conditions of the equipment. For such cases, it is effective to use active clamp circuits.

Fig. 5-9 shows an example of active clamp circuit. The circuit configuration adds a Zener diode at C-G of the IGBT, and connect a diode in anti-series with the Zener diode.

When voltage exceeding the Zener voltage of the Zener diode is applied on C-E, the Zener diode breakdown and current flows from collector to the IGBT gate. Positive voltage is added to V_{GE} by this current flowing through R_G. When V_{GE} exceeds the gate threshold voltage $V_{GE(th)}$, I_C flows through the IGBT, and V_{CE} is clamped to approximately equal to the Zener voltage of the Zener diode. In this way, surge voltage can be suppressed.

On the other hand, since the active clamp circuit turn on the IGBT, the di/dt at turn-off becomes slower than before the addition of the clamp circuit, resulting in a longer turn-off time (refer to Fig. 5-10). As this will increase the switching loss, make sure to apply the clamp circuit after verifying if this has no problem with the design of the equipment.

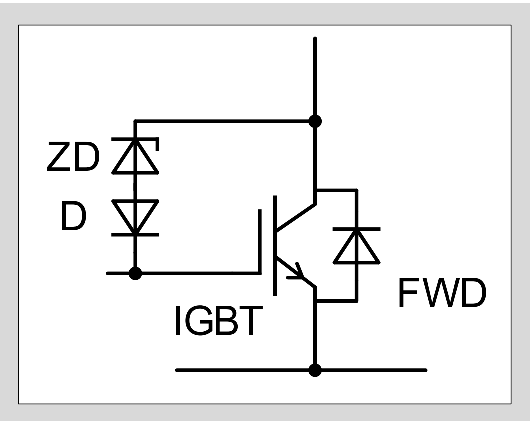

Fig. 5-9 Active clamp circuit

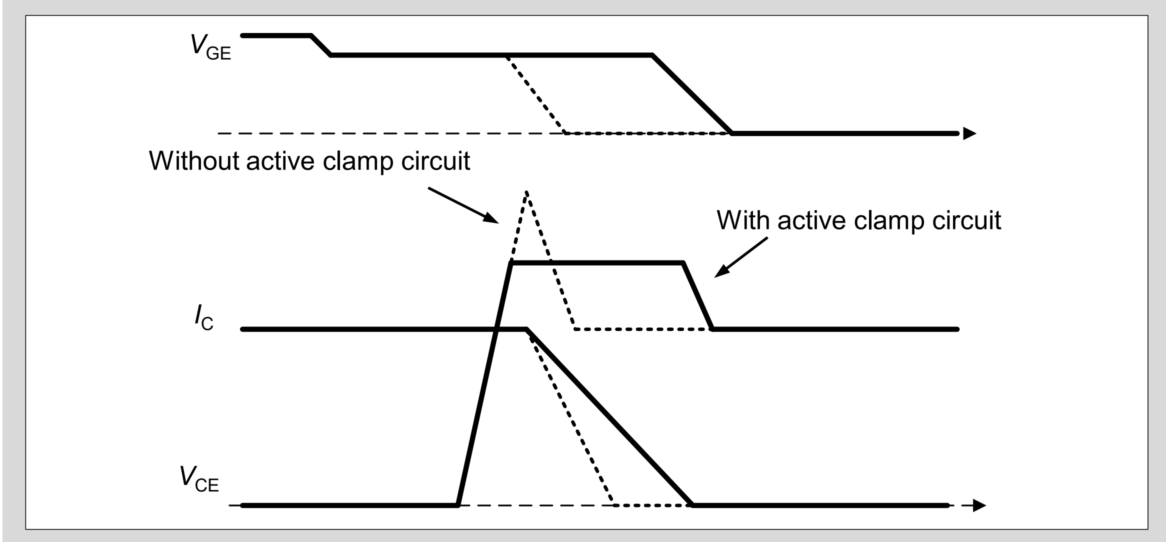

Fig. 5-10 Waveform example when active clamp circuit is applied

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Chapter 6 Cooling Design

1. Power Loss of Discrete IGBT	6-2
2. About Fuji IGBT Simulator	6-3
3. Power Loss Calculation Method of Boost Chopper Circuit	6-4
4. Power Loss Calculation Method of 3-phase 2-level PWM Inverter Circuit	6-5
5. Concept of Cooling Design	6-9

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1. Power Loss of Discrete IGBT

Discrete IGBTs are available in two types: IGBT only products and products that combine an IGBT with a freewheeling diode (FWD). For the latter, total loss must account for both the IGBT's loss and the FWD's loss. As shown in Fig. 6-1, power loss are divided into conduction loss and switching loss. The types of power loss is summarized in Fig. 6-2.

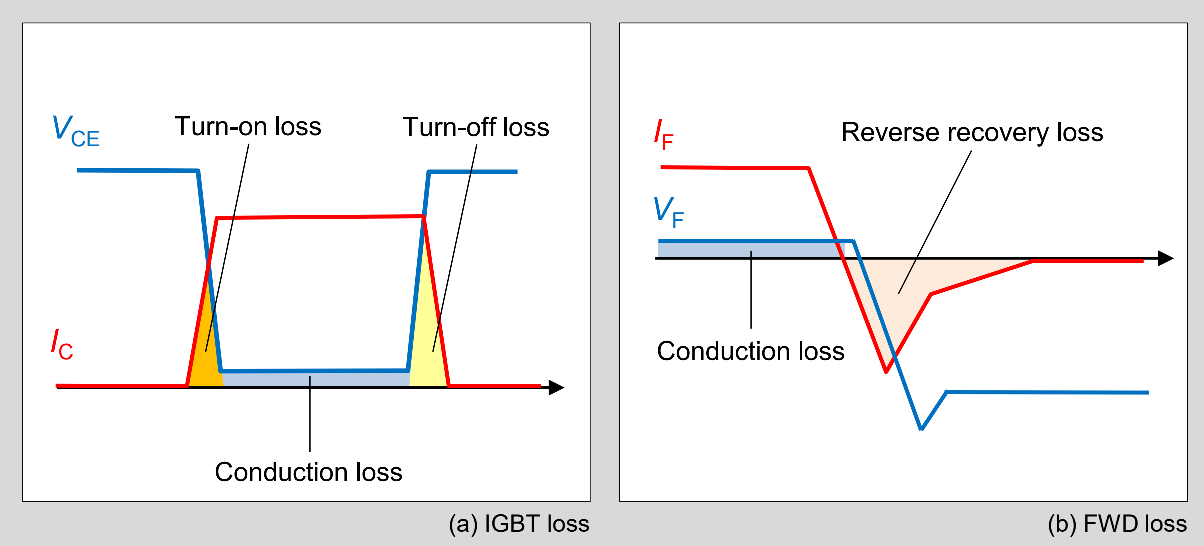

Fig. 6-1 Switching waveform and power loss of IGBT and FWD

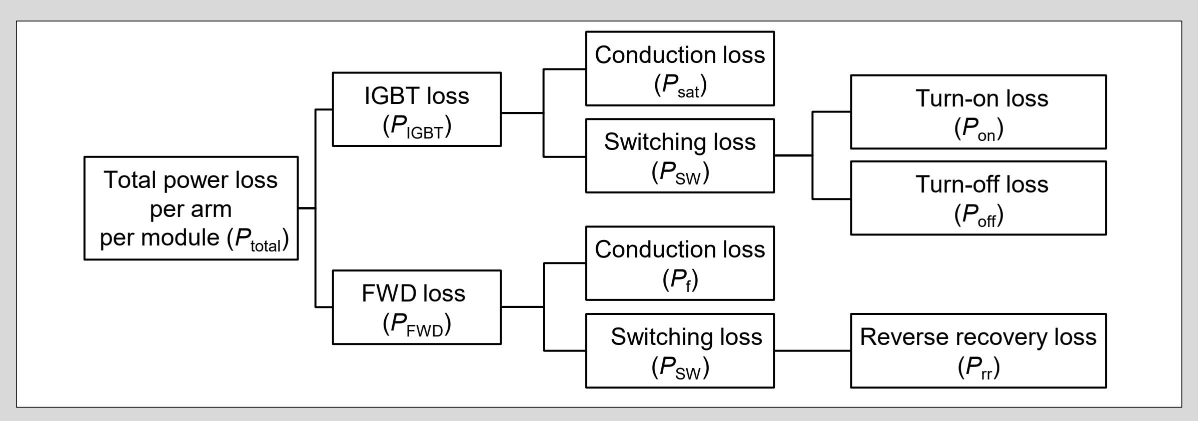

Fig. 6-2 Classification of IGBT module power loss

The conduction loss of the IGBT part is calculated from the $V_{CE(sat)}$ -I_C characteristic, and the conduction loss of the FWD part is calculated from the V_F-I_F characteristic shown in the datasheet. In addition, each switching loss is calculated from the E_{on}-I_C, E_{off}-I_C, E_{rr}-I_F characteristics. Cooling design is performed based on these power loss so that the T_{vj} of the IGBT and FWD do not exceed the temperature rating. Therefore, calculate the power loss using the data when T_{vj} is high.

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2. About Fuji IGBT Simulator

On our website, we provide the “Fuji IGBT Simulator” as a tool for calculating the power loss and junction temperature of discrete IGBTs. This simulator performs calculation by accurately fitting the characteristic curves from the datasheet, and also in consideration of the device’s junction temperature dependence. For instructions on how to use it, please refer to the user manual available on the website.

However, some products or circuit configurations may not be supported by the Fuji IGBT Simulator. In those cases, you will need to perform the loss calculations manually. In the following sections, we describe the methods for calculating each type of power loss.

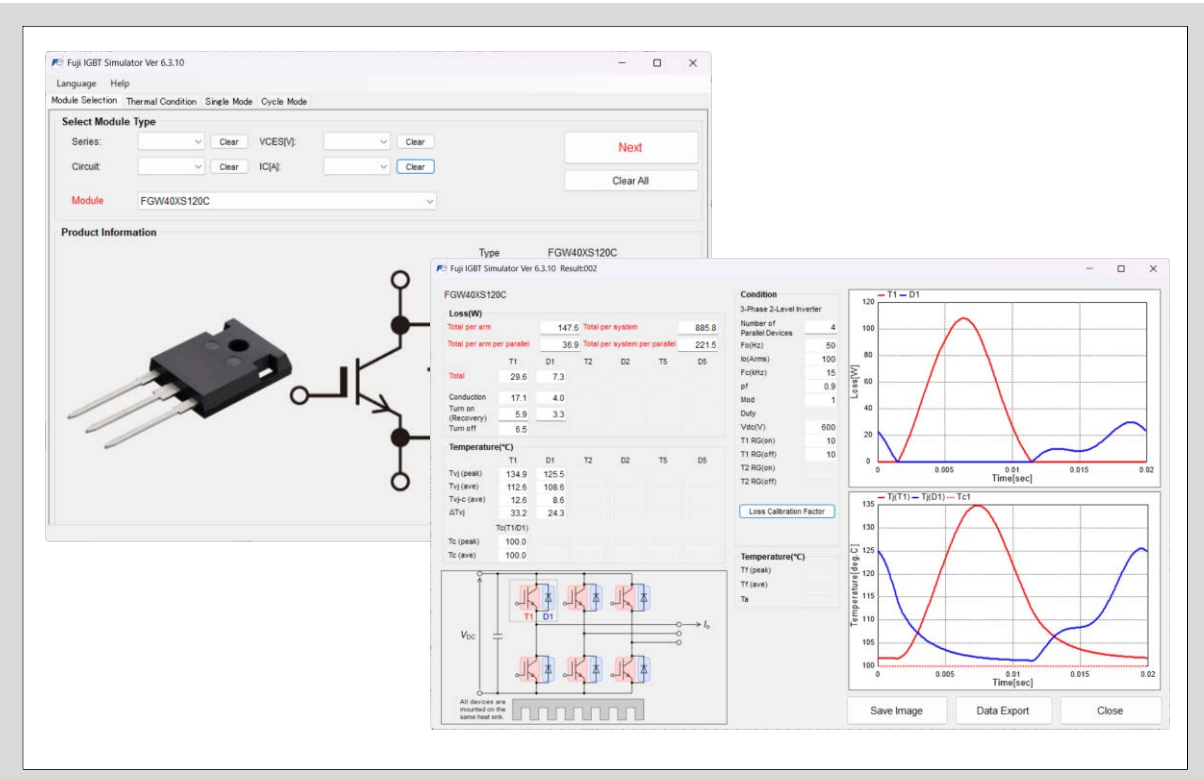

Fig. 6-3 Fuji IGBT Simulator

Fuji IGBT Simulator：https://www.fujielectric.com/products/semiconductor/model/igbt/simulation/

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3. Power Loss Calculation Method of Boost Chopper Circuit

In the case of a boost chopper circuit as shown in Fig. 6-4, if the current flowing through the IGBT (T_1) and FWD (D_1) is considered to be a continuous rectangular waveform, the power loss per unit time of T_1 and D_1 (unit: W) can be approximated by the following formulas.

P_{IGBT} = Conduction loss + Turn-on loss + Turn-off loss

$$= V_{CE(sat)} \cdot I_C \cdot d + (E_{on} + E_{off}) \cdot f_C \cdot (\frac{V_{cc}}{V_{cc0}})^{\alpha} \quad \text{..........(1)}$$

P_{FWD} = Conduction loss + Reverse recovery loss

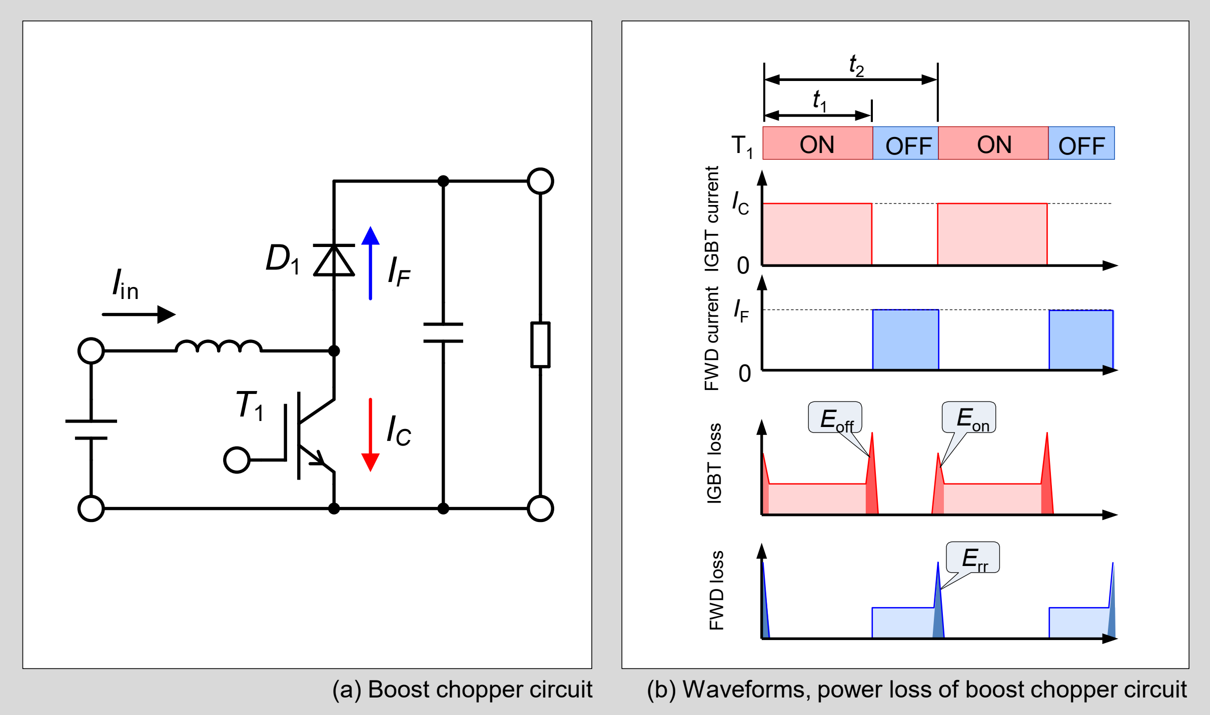
$$= V_F \cdot I_F \cdot (1-d) + E_{rr} \cdot f_C \cdot (\frac{V_{CC}}{V_{CC0}})^{\alpha} \quad \text{..........(2)}$$

where

d	:IGBT ON duty= t_1 / t_2
f_c	:Switching frequency = 1 / t_2
V_{CC}	:Switching voltage
V_{CC0}	:Switching voltage of switching loss data in datasheet
α	:Coefficient of switching voltage dependence to switching energy

If we consider the switching energy to be proportional to the switching voltage, then we can set α=1.

On the other hand, the values of $V_{CE(sat)}$, V_F, E_{on}, E_{off}, and E_{rr} depend on the junction temperature T_{vj} of the device. Thus, if the T_{vj} is different from the T_{vj} described in the datasheet, refer to the T_{vj} dependency graphs in the datasheet for conversion. The values of E_{on}, E_{off}, and E_{rr} also depend on the gate resistance value R_G, so refer to the R_G dependency graph in the datasheet for conversion.



(a) Boost chopper circuit (b) Waveforms, power loss of boost chopper circuit

Fig. 6-4 Power loss in boost chopper circuit

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4. Power Loss Calculation Method of 3-phase 2-level PWM Inverter Circuit

As shown in Fig. 6-5, the current values of the IGBT and FWD in a 3-phase 2-level PWM inverter are constantly changing. Thus, an accurate calculation of the power loss requires complex calculations. Here, we introduce a simple method for calculating the power loss of the IGBT and FWD in an inverter circuit using the characteristic curve approximation formula of the IGBT module.

The following conditions are assumed for the calculation.

- The inverter is a PWM controlled 3-phase 2-level inverter
- PWM is triangle wave comparison sinusoidal modulation method
- The output current should be an ideal sine wave

Assuming that the RMS value of the output phase current of the inverter is I_o, the current waveform of the sine wave is expressed by the following formula.

$$i_O(\theta) = \sqrt{2} \cdot I_O \cdot \sin\theta \quad \cdots\cdots(3)$$

The on-duty waveform $d(\theta)$ of the IGBT is expressed by the following formula, where m is the modulation factor and φ is the delay power factor of the current.

$$d(\theta) = \frac{1 + m \cdot \sin(\theta + \varphi)}{2} \quad \cdots\cdots(4)$$

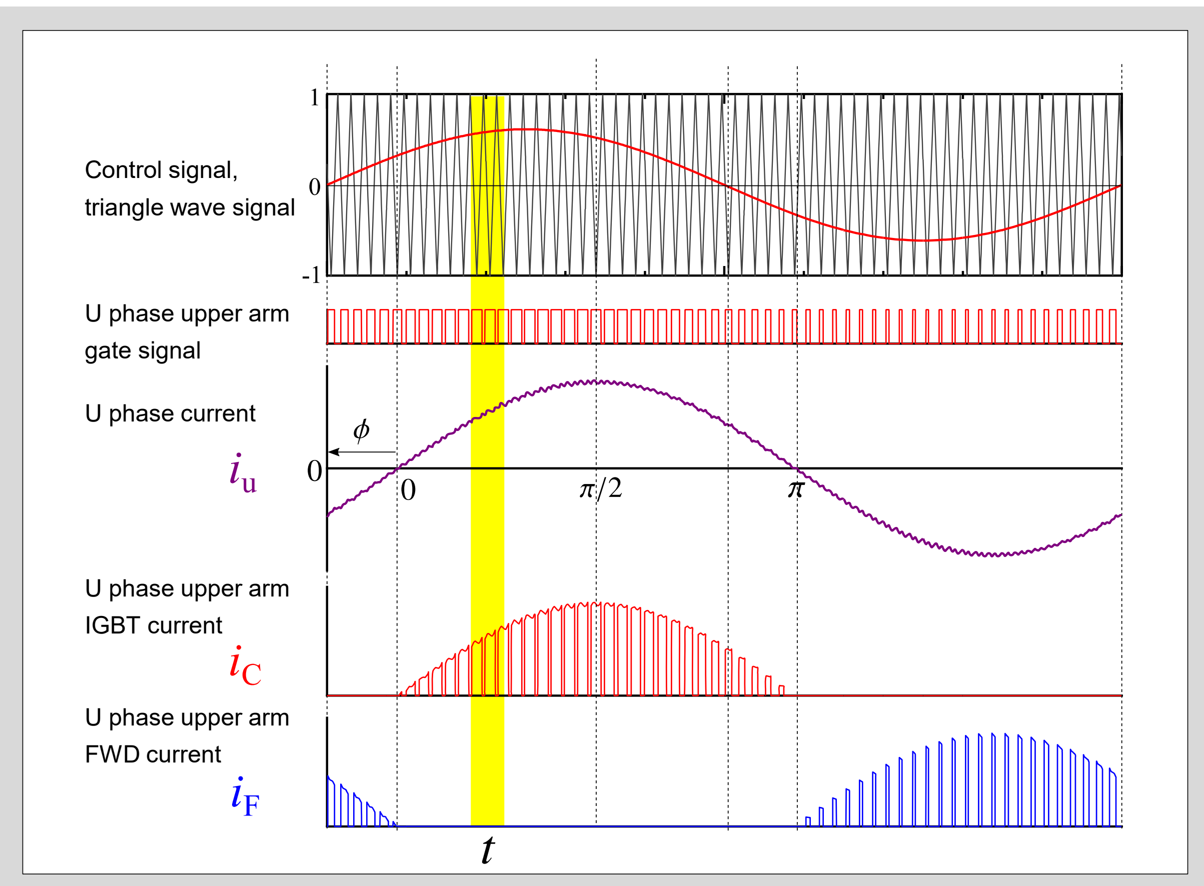

Fig. 6-5 Operating waveform of a 3-phase 2-level PWM inverter

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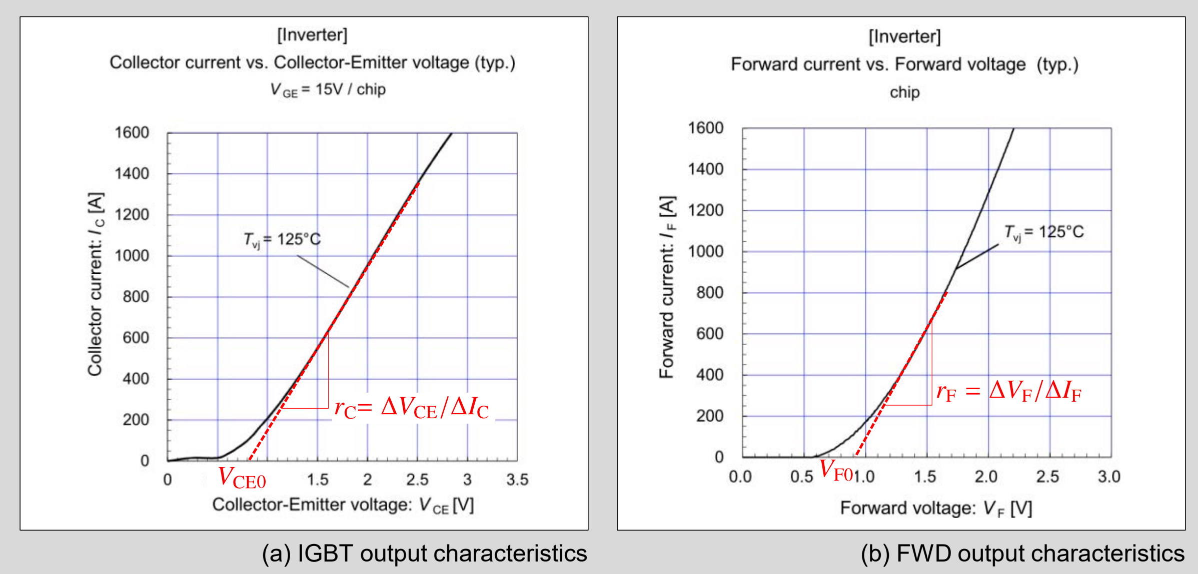
When I_C flows through the IGBT, Collector-Emitter saturation voltage $V_{CE(sat)}$ is generated. $V_{CE(sat)}$ value depends on I_C, and the $V_{CE(sat)}$- I_C graph is shown in the datasheet. In order to calculate the conduction loss of the IGBT, the I_C dependence of $V_{CE(sat)}$ is linearly approximated as shown in Fig. 6-6, and is expressed by the following formula.

$$V_{CEsat} = r_C \cdot I_C + V_{CEO} \qquad \text{(5)}$$

Similarly, the I_F dependence of FWD forward voltage V_F is expressed by the following formula when linearly approximated.

$$V_F = r_F \cdot I_F + V_{FO} \qquad \text{(6)}$$



(a) IGBT output characteristics (b) FWD output characteristics

Fig. 6-6 Linear approximation of output characteristics

From formula (3), (4) and (5), the IGBT conduction loss P_{sat} per arm is calculated as follows.

$$P_{sat} = \frac{1}{2\pi}\int_0^{\pi}\{i_O(\theta)\cdot V_{CEsat}(\theta)\cdot d(\theta)\}d\theta$$

$$= 2I_O^2 \cdot rc\left(\frac{1}{8}+\frac{m}{3\pi}\cos\varphi\right)+\sqrt{2}\cdot I_O\cdot V_{CEO}\left(\frac{1}{2\pi}+\frac{m}{8}\cos\varphi\right) \qquad \text{(7)}$$

Similarly, the FWD conduction loss P_f per arm is calculated as follows.

$$P_f = \frac{1}{2\pi}\int_{\pi}^{2\pi}\{-i_O(\theta)\cdot V_F(\theta)\cdot d(\theta)\}\,d\theta$$

$$= 2I_O^2 \cdot r_F\left(\frac{1}{8}-\frac{m}{3\pi}\cos\varphi\right)+\sqrt{2}\cdot I_O\cdot V_{FO}\left(\frac{1}{2\pi}-\frac{m}{8}\cos\varphi\right) \qquad \text{(8)}$$

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Next, in order to calculate the switching loss, the approximate expression of the I_C dependence graph of E_{on}, E_{off}, and E_{rr} described in the datasheet are obtained. As shown in Fig. 6-7, if the I_C dependence curve of the switching energy is linearly approximated, and the coefficient of switching voltage dependence is set as α = 1, E_{on}, E_{off}, and E_{rr} can be expressed by the following formulas, respectively.

$$E_{on}(I_C) = k_{on} \cdot I_C \cdot \left(\frac{V_{CC}}{V_{CC0}}\right) \quad \text{(9)}$$

$$E_{off}(I_C) = k_{off} \cdot I_C \cdot \left(\frac{V_{CC}}{V_{CC0}}\right) \quad \text{(10)}$$

$$E_{rr}(I_F) = k_{rr} \cdot I_F \cdot \left(\frac{V_{CC}}{V_{CC0}}\right) \quad \text{(11)}$$

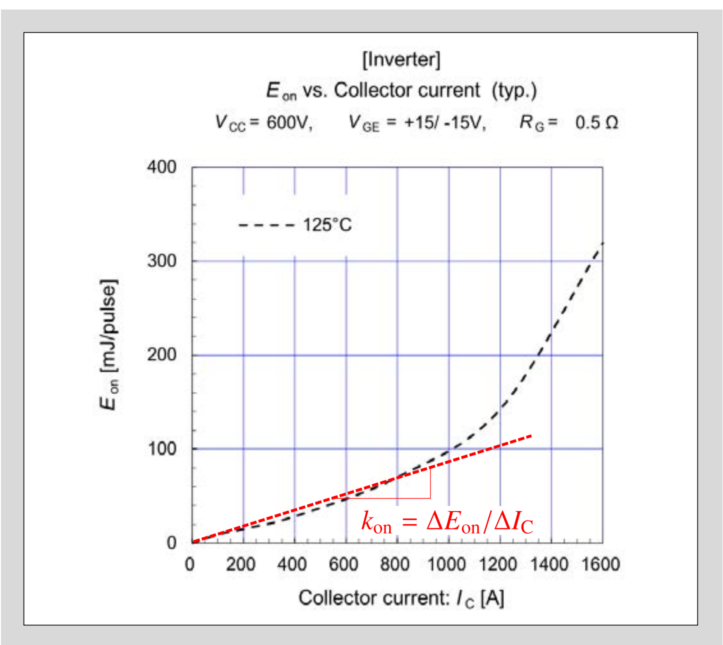

Fig. 6-7 Approximation of I_C dependence of switching energy

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Using formula (9), the IGBT turn-on loss P_{on} per arm can be calculated by the following formula.

$$P_{on} = \frac{1}{2\pi}\int_0^{\pi}\left\{k_{on}(\sqrt{2}\cdot I_o \cdot \sin\theta)\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW}\right\}d\theta$$

$$= \frac{\sqrt{2}}{\pi}k_{on}\cdot I_O\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW} \quad \text{……(12)}$$

Similarly, the IGBT turn-off loss P_{off} and the FWD reverse recovery loss P_{rr} can be calculated by the following formulas, respectively.

$$P_{off} = \frac{\sqrt{2}}{\pi}\cdot k_{off}\cdot I_O\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW} \quad \text{……(13)}$$

$$P_{rr} = \frac{\sqrt{2}}{\pi}\cdot k_{rr}\cdot I_O\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW} \quad \text{……(14)}$$

From the above calculation, the IGBT power loss P_{IGBT} and the FWD power loss P_{FWD} per arm can be calculated as follows, respectively.

$$P_{IGBT} = P_{sat} + P_{on} + P_{off} \quad \text{……(15)}$$

$$P_{FWD} = P_f + P_{rr} \quad \text{……(16)}$$

As mentioned, since the values of $V_{CE(sat)}$, V_F, E_{on}, E_{off}, and E_{rr} change depending on T_{vj} and R_G, refer to the T_{vj} and R_G dependency graphs in the datasheet for conversion when calculating.

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5. Concept of Cooling Design

In cooling design, the heat sink is selected based on the calculated power loss so that the device temperature stays below its allowable limit. If the cooling design is inadequate, there is a risk that the device may exceed its maximum junction temperature during actual operation and fail.

5.1 Transient thermal impedance and steady-state thermal resistance

When mounting the device on a heat sink, the heat dissipation path for power loss generated at the junction is modeled by the equivalent electrical circuit as shown in Fig. 6-8.

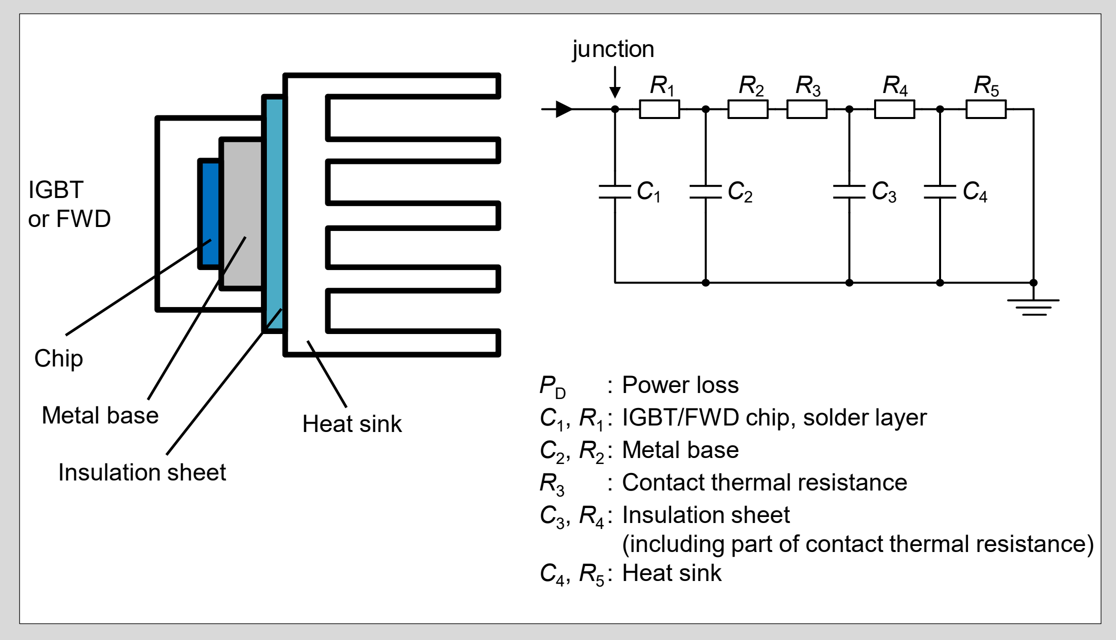

Fig. 6-8 Equivalent electrical circuit of thermal behavior

Transient thermal impedance, as modeled by the equivalent circuit in Fig. 6-8, is the impedance over the time range in which the thermal capacitances C1-C4 have influences, and is therefore a function of time. The transient thermal impedance characteristic of each device has its maximum value specified in the datasheet, corresponding to a duty cycle D ≅ 0. The transient thermal impedance of the heat sink can be calculated from the following equation.

$$R_{f(t)} = R_{th(f-a)}\left(1 - e^{-\frac{t}{\tau f}}\right)$$

where, $\tau f = R_{th(f-a)} \cdot V \cdot \gamma \cdot C$

$R_{th(f-a)}$: Steady-state thermal resistance of the heat sink [°C/W]
t : Time [s]
τf : Thermal time constant of the heat sink [s]
V : Heat sink volume [cm^3]
γ : Density [g/cm^3]
C : Specific heat [J/g·deg]

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The densities and specific heats of the materials required for these calculations are listed in Table 6-1, and the steady-state thermal resistance of the aluminum heat sink is shown in Fig. 6-9.

Table 6-1 Density and specific heat of each material

Material	Density γ [g/cm^3]	Specific heat [J/g･deg]
Aluminum	2.71	0.895
Cooper	8.96	0.383

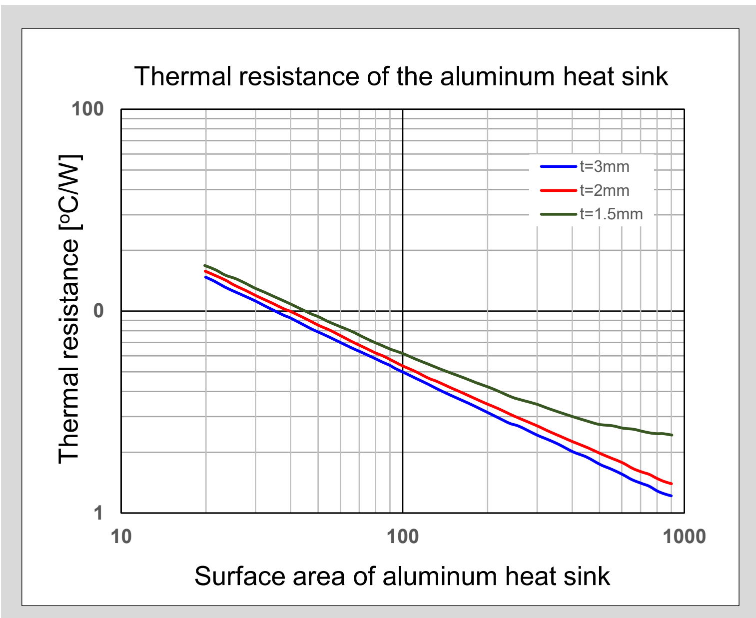

Fig. 6-9 Steady-state thermal resistance of the aluminum heat sink

5.2 Steady-State thermal equation

The steady-state thermal resistance is the thermal resistance when the influences of thermal capacitances have completely disappeared. The device's junction temperature can then be easily calculated.

$$T_{vj} = T_a + P_D \cdot (R_{th(j\text{-}c)} + R_{th(c\text{-}i)} + R_{th(i)} + R_{th(i\text{-}f)} + R_{th(f\text{-}a)})$$

T_{vj} : Junction temperature
T_a : Ambient temperature
$R_{th(j\text{-}c)}$: Junction to case thermal resistance (IGBT or FWD)
$R_{th(i)}$: Insulation sheet thermal resistance
$R_{th(c\text{-}i)}$, $R_{th(i\text{-}f)}$: Contact thermal resistance
$R_{th(f\text{-}a)}$: Heat sink thermal resistance
P_D : Power loss

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5.3 Thermal equations for transient state

In general, it is sufficient to consider the steady-state T_{vj} from the average power loss. However, in reality, repetitive switching operation generates power loss in pulse and cause temperature ripples as shown in Fig. 6-11. In this case, if the power loss is considered as a continuous rectangular wave with constant period and constant peak value, the peak value of the temperature ripples T_{vjp} can be approximated with the following formula using the transient thermal resistance curve described in the datasheet (Fig. 6-10).

Select a heat sink by confirming that T_{vjp} does not exceed $T_{vj\ (max.)}$.

$$T_{jp} - T_C = P \cdot \left[R(\infty) \cdot \frac{t1}{t2} + \left(1 - \frac{t1}{t2}\right) \cdot R(t1 + t2) - R(t2) + R(t1) \right]$$

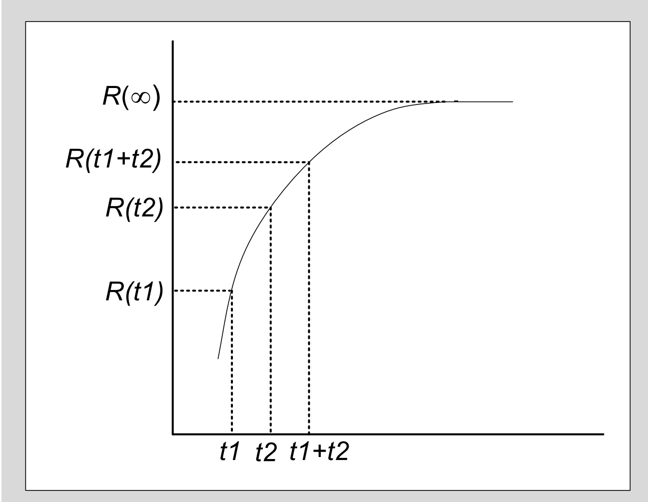

Fig. 6-10 Transient thermal resistance curve

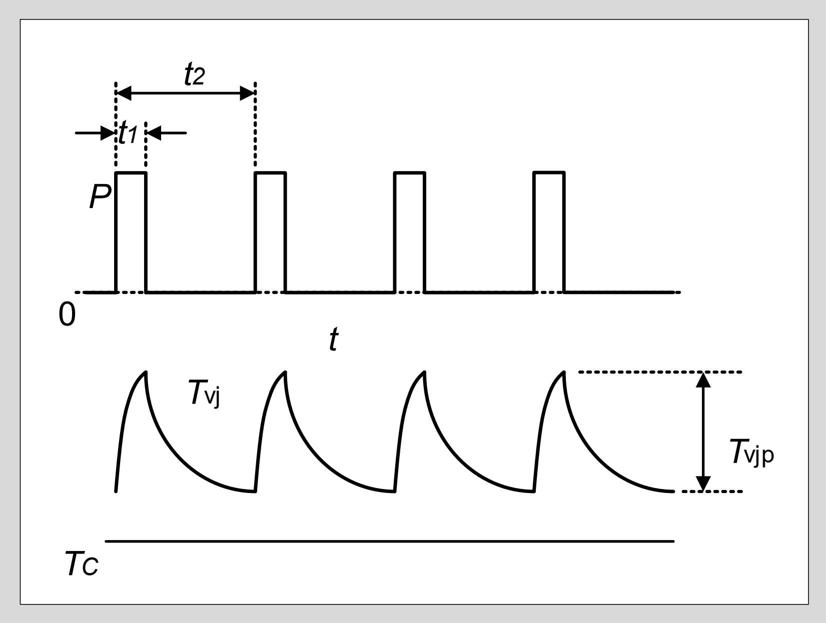

Fig. 6-11 Thermal ripples

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Chapter 7 Gate Drive Circuit Design

1. IGBT Gate Drive Conditions and Main Characteristics	7-2
2. Drive Current	7-6
3. Setting Dead Time	7-7
4. Examples of Gate Drive Circuits	7-9
5. Precautions for Gate Drive Circuit Design	7-10

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This chapter describes about the gate drive circuit design.

1. IGBT Gate Drive Conditions and Main Characteristics

Table 7-1 shows the general relationship between the gate drive conditions and the main characteristics of the IGBT. Since the main characteristics of the IGBT change depending on V_{GE} and R_G, it is necessary to set them according to the design goal of the equipment.

Table 7-1 IGBT drive conditions and main characteristics

Main characteristics	$+V_{GE}$ increase	$-V_{GE}$ increase	$R_{G(ON)}$ increase	$R_{G(OFF)}$ increase
$V_{CE(sat)}$	↓	–	–	–
t_{on} E_{on}	↓	–	↑	–
t_{off} E_{off}	–	↓	–	↑
Turn-on FWD surge voltage	↑	–	↓	–
Turn-off IGBT surge voltage	–	↑	–	↓ *1
dv/dt malfunction	↑	↓	↓	↓
Saturation current	↑	–	–	–
Short circuit withstand capability *2	↓	–	–	–
Radiation noise	↑	–	↓	↓

*1: Gate resistance dependence of surge voltage is different for each series
*2: Short circuit withstand capability is not guaranteed for the XS series.

1.1 Gate forward bias voltage $+V_{GE}$ (On state)

The recommended value for $+V_{GE}$ is +15V. Notes when designing $+V_{GE}$ are shown as follows.

- Set $+V_{GE}$ so that it remains below the maximum G-E rated voltage of ±20V.
- It is recommended that supply voltage fluctuations are kept within ±10%.
- The $V_{CE(sat)}$ is inversely proportional to $+V_{GE}$, so the higher the $+V_{GE}$ the smaller the $V_{CE(sat)}$.
- The higher the $+V_{GE}$, the shorter the turn-on switching time (smaller turn-on loss).
- The higher the $+V_{GE}$, the larger the opposing arm FWD reverse recovery surge voltage.
- Even while the IGBT is in the off-state, there may be malfunction due to dv/dt during FWD reverse recovery, causing pulsed short circuit current to flow and resulting in excessive heat generation. In the worst case, the module might be destroyed. This phenomenon is called a dv/dt shoot-through and is more likely to occur when $+V_{GE}$ is higher.
- The higher the $+V_{GE}$, the higher the saturation current.

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1.2 Gate reverse bias voltage -V_{GE} (Off state)

The recommended value for -V_{GE} is –5 to -15V. Notes when designing -V_{GE} are shown as follows.

- Set -V_{GE} so that it remains below the maximum G-E rated voltage of ±20V.
- It is recommended that supply voltage fluctuations are kept within ±10%.
- The IGBT turn-off characteristics depend on -V_{GE}, especially the characteristics of the part where the collector current I_C begins to turn off strongly depend on -V_{GE}. Therefore, the higher the -V_{GE}, the shorter the turn-off switching time (smaller turn-off loss).

1.3 Gate resistance R_G

The R_G listed in the product datasheets is the value that minimizes the switching losses within the absolute maximum ratings under Fuji's measurement environment. Thus, R_G must be changed appropriately according to the circuit and operating conditions. Notes when designing R_G are shown as follows.

- The switching characteristics of both turn-on and turn-off are dependent on the value of R_G. The larger the R_G, the longer the switching time and the greater the switching loss. On the other hand, although generally the surge voltage during turn-off switching decreases as R_G increases, surge voltage may increase as R_G increases depending on the device structure. Refer to technical documents for details. Technical documents are available for each IGBT series and voltage rating.
- The larger the R_G, dv/dt shoot-through is less likely to occur.
- Various switching characteristics vary greatly due to stray inductance in the circuit. In particular, the surge voltage during IGBT turn-off and FWD reverse recovery are greatly affected by stray inductance. Therefore, minimize the stray inductance when designing R_G.

Select the most suitable gate drive conditions while paying attention to the above points.

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1.4 Countermeasures of d*v*/d*t* induced false turn-on

In this section, we explain the mechanism by which the IGBT can undergo a gate false turn-on due to the d*v*/d*t* generated during the FWD's reverse recovery, and the countermeasures.

Fig. 7-1 shows the principle of d*v*/d*t* induced false turn-on. In this figure, it is assumed that IGBT1 transition from off state to on state, and V_{GE} of IGBT2 is reverse biased. In this condition, when IGBT1 turns on, reverse recovery of FWD2 happens. At the same time, the voltage across IGBT2 (FWD2) rises, generating d*v*/d*t* according to the turn-on of IGBT1. Because IGBT1 and IGBT2 have feedback capacitance C_{res}, current $I=C_{res}$ x d*v*/d*t* flows through C_{res}. V_{GE} of IGBT2 rises as this current flows through R_G. When V_{GE} exceeds the sum of the reverse biased voltage and gate threshold voltage $V_{GE(th)}$ of IGBT2, IGBT2 is turned on, resulting in short circuit of IGBT1 and IGBT2.

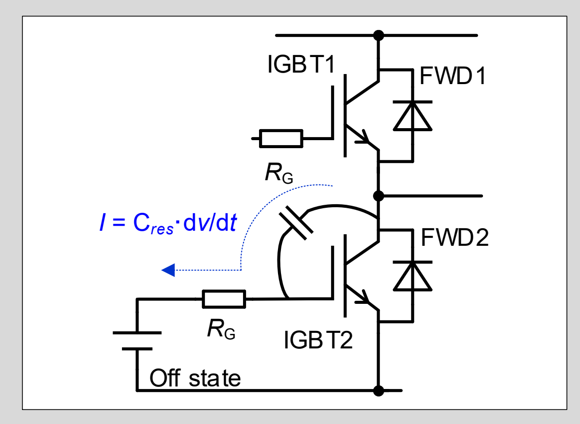

Fig. 7-1 Principle of d*v*/d*t* induced false turn-on

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Based on this principle, countermeasures are shown in Fig. 7-2. There are three methods, which are (a) adding C_{GE} to suppress the transient rise of V_{GE}, (b) increase -V_{GE} to lower the transient peak value of V_{GE}, and (c) increase R_G to lower dv/dt. The effectiveness of these countermeasures vary depending on the gate drive circuit, thus be sure to evaluate them thoroughly. Note that these countermeasures also affect switching loss, so be sure to consider this as well.

The aim of adding C_{GE} is to reduce the current flowing through R_G by bypassing to C_{GE}. However, by adding C_{GE}, it is necessary to charge this C_{GE} when driving the gate, which reduces the switching speed and increase the switching loss. This can be adjusted by lowering the R_G value. In other words, by selecting an appropriate combination of C_{GE} and R_G, it is possible to avoid dv/dt induced false turn-on without increasing switching loss. As a guideline, the recommended C_{GE} value is about twice the C_{ies} value shown in the datasheet, and the recommended R_G value is about half the value before adding C_{GE}. Connect C_{GE} as close as possible to the G-E terminals. Confirm the selection of C_{GE} and R_G by actual evaluation.

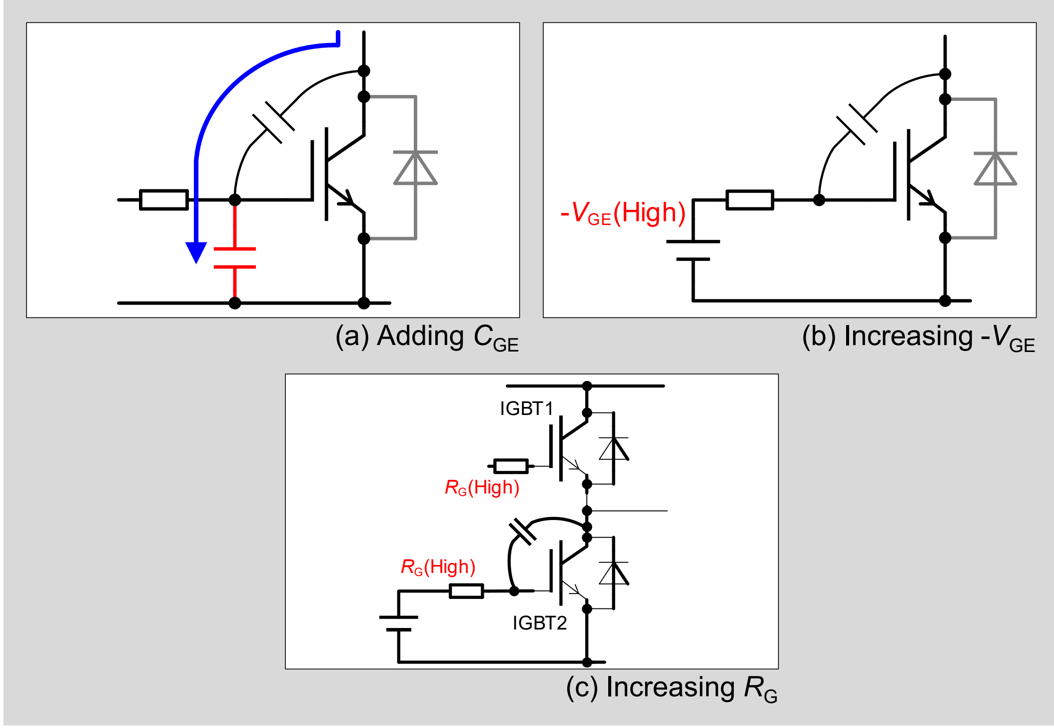

Fig. 7-2 Countermeasures against dv/dt induced false turn-on

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2. Drive Current

Since IGBT has a MOS gate structure, drive current is needed to charge and discharge this gate during switching. Fig. 7-3 shows the gate charge (dynamic input) characteristics. The gate charge characteristics show the amount of charge required to drive the IGBT and can be used to calculate the average drive current and drive power. Fig. 7-4 shows the gate drive circuit schematic, as well as the gate voltage V_{GE} and drive current I_G waveforms. The principle of the gate drive circuit is to switch alternately between the forward bias and reverse bias power supply using switch S_1 and S_2. During switching, the drive current is used to charge and discharge the gate. The area (shaded) under the drive current waveform in Fig. 7-4 is equal to the gate charge shown in Fig. 7-3.

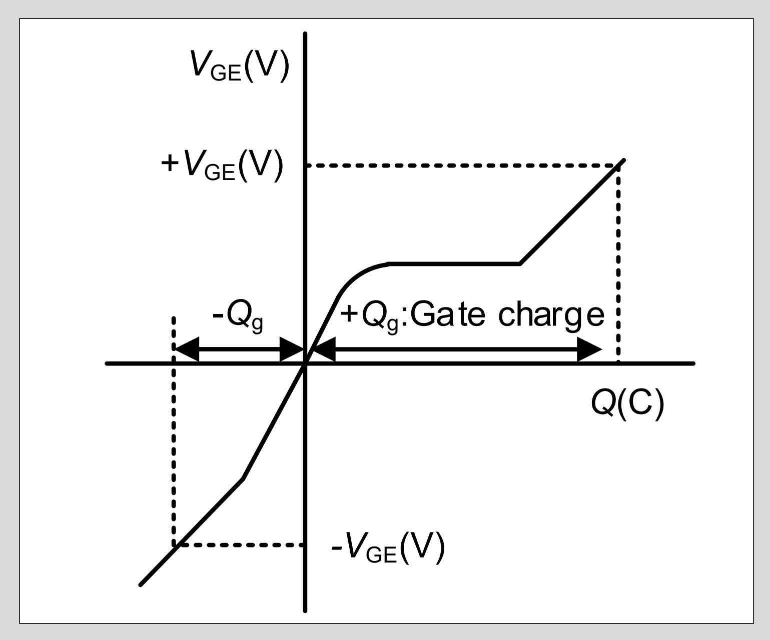

Fig. 7-3 Gate charge (Dynamic input) characteristics

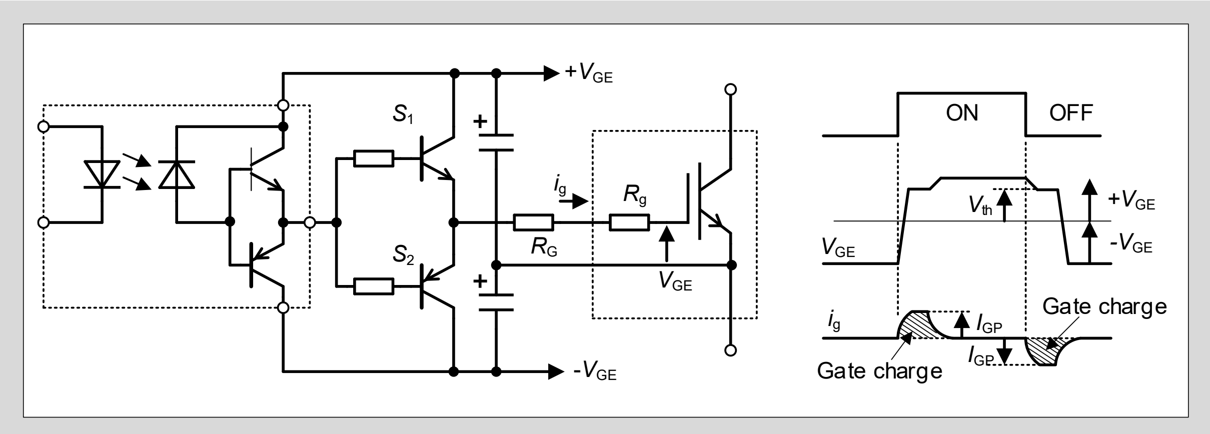

Fig. 7-4 Gate drive circuit schematic and waveforms

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The drive current peak value I_{GP} can be approximately calculated as follows.

$$I_{GP} = \frac{+V_{GE} + |-V_{GE}|}{R_G}$$

$+V_{GE}$:Forward bias supply voltage
$-V_{GE}$:Reverse bias supply voltage
R_G :Gate resistance

Internal gate resistance r_g differs for each product. Thus, refer to the datasheet of each product.

On the other hand, the average value of the drive current I_G can be calculated by the following formula using the gate charge characteristics (Fig.7-3).

$$+I_G = -I_G = f_C \cdot \left(\left|+Q_g\right| + \left|-Q_g\right|\right)$$

f_c :Switching frequency
$+Q_g$:Gate charge from 0V to $+V_{GE}$
$-Q_G$:Gate charge from $-V_{GE}$ to 0V

Furthermore, if all the power loss of the gate drive circuit is consumed by R_G, the drive power P_d required to drive the IGBT is shown by the following formula.

$$P_{d(on)} = f_C \cdot \left[\frac{1}{2}\left(\left|+Q_g\right| + \left|-Q_g\right|\right) \cdot \left(|+V_{GE}| + |-V_{GE}|\right)\right]$$

$$P_{d(off)} = P_{d(on)}$$

$$P_d = P_{d(off)} + P_{d(on)}$$

$$= f_C \cdot \left(\left|+Q_g\right| + \left|-Q_g\right|\right) \cdot \left(|+V_{GE}| + |-V_{GE}|\right)$$

Therefore, it is necessary to select R_G with proper power rating according to P_d.

Be sure to design the gate drive circuit so that the above-mentioned drive current and drive power can be properly supplied.

3. Setting Dead time

In inverter circuits, etc., it is necessary to set an on-off timing delay (dead time) in order to prevent short circuits between the upper and lower arms. As shown in Fig. 7-5, both the upper and lower arms are in the off state during the dead time.

Basically, the dead time needs to be set longer than the IGBT switching time ($t_{off\ max}$.). For example, if R_G is increased, switching time also becomes longer, so the dead time must be increased as well. Also, it is necessary to consider other drive conditions and temperature characteristics. If the dead time is too short, short circuit between the upper and lower arms may occur, and the heat generated by the short circuit current may destroy the module. A dead time of 3μsec or more is recommended for IGBT modules. Check if the dead time is sufficient by doing actual evaluation.

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One method of determining whether the dead time setting is sufficient is to check the current in the DC power line at no load condition.

In the case of a 3-phase inverter, set the inverter outputs (U, V, W) to open, apply normal input signals, and measure the DC power line current as shown in Fig. 7-6. Even if the dead time is sufficient, a very small pulse current (dv/dt current through the device output capacitance: about 5% of the rated current) will be observed. However, if the dead time is insufficient, a large short circuit current will be observed. In this case, increase the dead time until the short circuit current disappears. It is recommended to perform this test at high temperature as the turn-off time is longer. Short circuit current also increases if the gate reverse bias voltage -V_{GE} is insufficient (refer to Chapter 4, section 3.2). Increase -V_{GE} if increasing the dead time does not reduce the short circuit current. -V_{GE} of 5V and above is recommended.

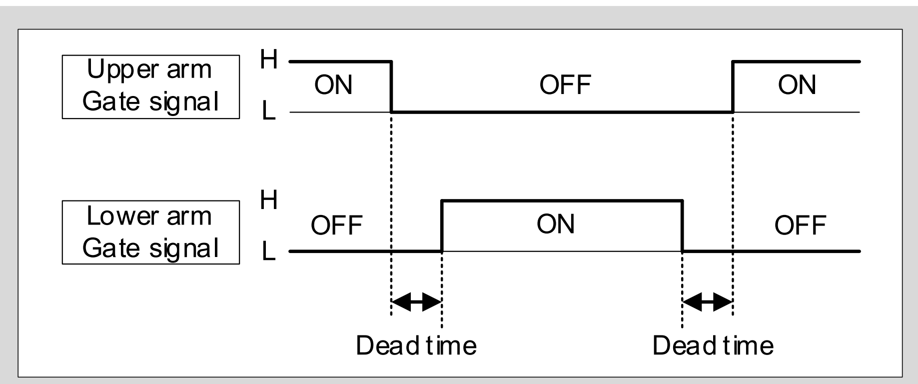

Fig. 7-5 Dead time timing chart

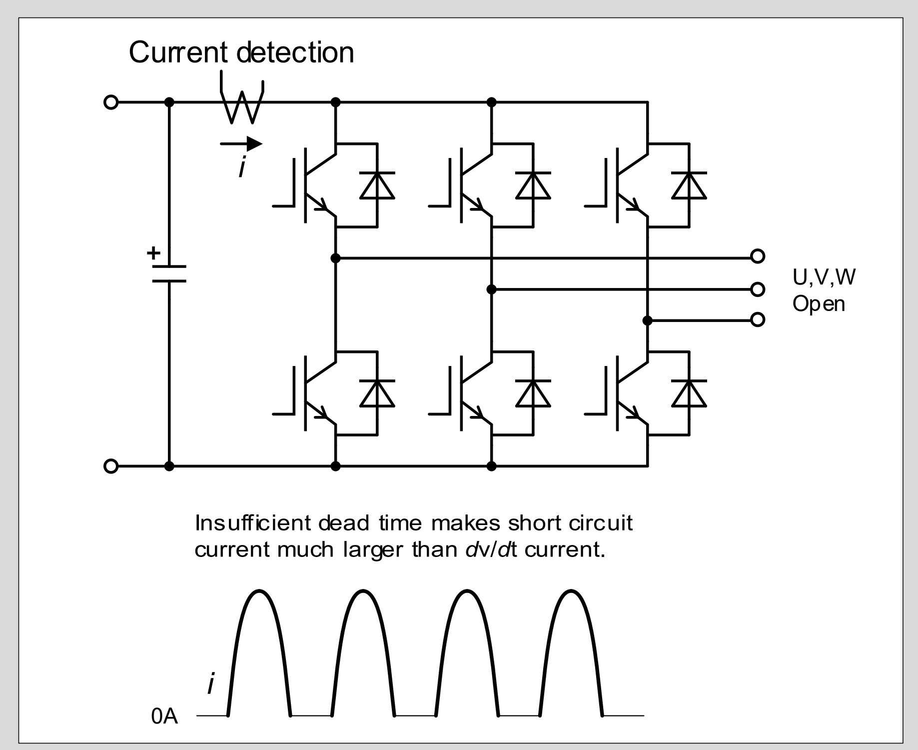

Fig. 7-6 Method for detecting short circuit current due to insufficient dead time

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4. Example of Gate Drive Circuits

In inverter circuits, etc., it is necessary to electrically isolate the main circuit and the control circuit. Fig. 7-7 shows an example of a gate drive circuit using high speed optocoupler. By using optocoupler, the input signal and the module are electrically isolated from each other. Also, since optocouplers do not limit the output pulse width, they are suitable for applications where the signal pulse width varies over a wide range, such as PWM control, and is the most widely used.

In addition, turn-on and turn-off gate resistors can be used separately.

Furthermore, there is also a signal isolation method using a pulse transformer. This method can simplify the circuit because both the signal as well as the gate drive power can be supplied simultaneously from the signal side. However, this method have limitations such as a maximum duty ratio of 50%, and reverse bias cannot be set.

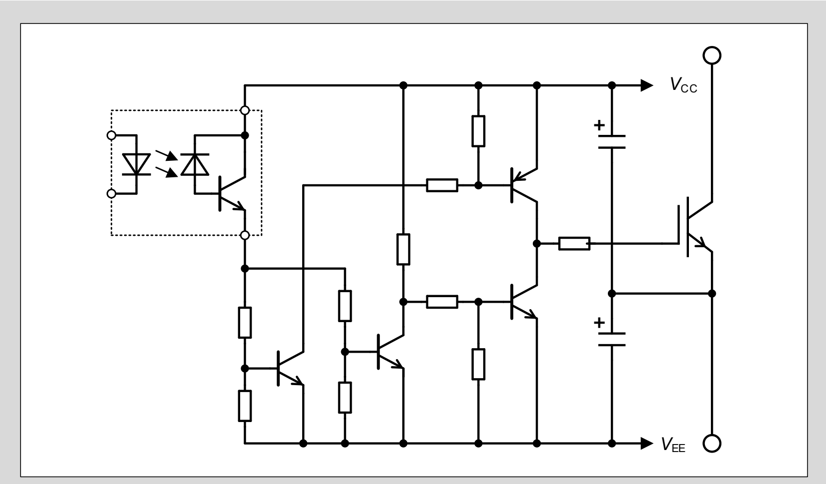

Fig. 7-7 Example of gate drive circuit using high speed optocoupler

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5. Precautions for Gate Drive Circuit Design

5.1 Optocoupler noise ruggedness

As IGBTs are high speed switching devices, it is necessary to select optocoupler for gate drive circuit that has high noise ruggedness. Also, to prevent malfunctions, make sure that the wiring from the optocoupler primary side and secondary side do not cross. Furthermore, in order to make full use of the IGBT high speed switching capability, using optocoupler with a short signal transmission delay is recommended.

5.2 Wiring between gate drive circuit and IGBT

If the wiring between the gate drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. There are the following countermeasures.

- Make the gate drive circuit wiring as short as possible, and use twisted pair wires for the gate and emitter wiring.
- Increase R_G. However, pay attention to the increase of switching time and switching loss.
- Separate the gate drive circuit and main circuit wiring as far as possible. If the wirings overlap, design the layout so that they cross each other (in order to avoid mutual induction).

*1 About R_{GE}

The IGBT may be destroyed if voltage is applied to the main circuit when the gate drive circuit is malfunctioned or not fully operating (gate in open state). In order to prevent this, it is recommended to connect a resistor R_{GE} of about 10kΩ between G-E (refer to Fig. 7-8).

When powering up, first turn on the gate drive circuit power supply. Switch on the main circuit power supply when the gate drive circuit is fully operational.

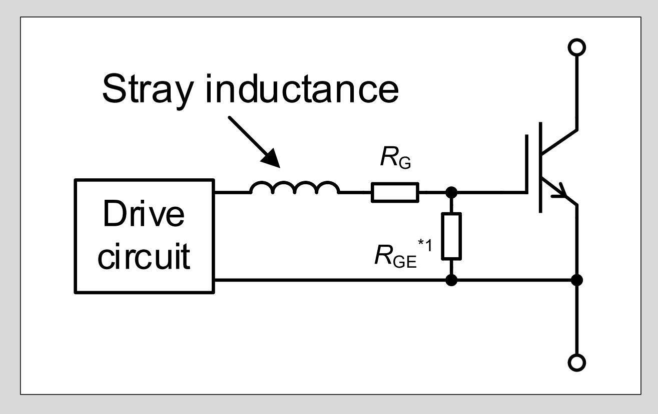

Fig. 7-8 Precautions for gate drive circuit design

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5.3 Gate overvoltage protection

It is necessary that IGBT modules, like other MOS devices, are sufficiently protected against static electricity. The G-E absolute maximum rated voltage is ±20V. If there is a possibility that a voltage exceeding this may be applied to G-E, protective measures such as connecting Zenner diode between G-E are required as shown in Fig. 7-9.

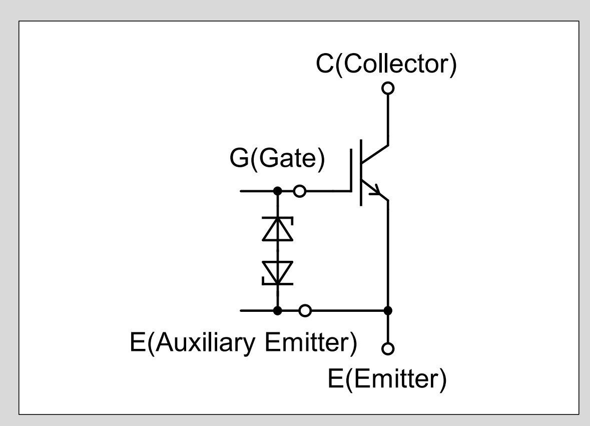

Fig. 7-9 G-E overvoltage protection circuit example

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Chapter 8 Parallel Connections

1. Selection of Discrete IGBTs 8-2
2. Main Circuit Design 8-6
3. Gate Drive Circuit Design 8-8
4. Cooling Design 8-11

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The IGBT current capacity can be increased by connecting discrete IGBTs in parallel. However, in this case, it is necessary to consider the current imbalance between the IGBTs, the temperature distribution, and the increase in noise and surge voltage due to the increase in wiring length.

Note the following points when connecting IGBTs in parallel.

1. Selection of IGBT
2. Main circuit design
3. Gate drive circuit design
4. Cooling design

This chapter describes the details of each point when connecting IGBTs in parallel.

1. Selection of Discrete IGBTs

Points to consider when connecting IGBTs in parallel are $V_{CE(sat)}$ variation ($\Delta V_{CE(sat)}$) and temperature dependent characteristic differences among the IGBTs on the same arm. Due to this $\Delta V_{CE(sat)}$, that is, the difference in the output characteristics of each IGBT, current imbalance occurs in the steady-state. If this current imbalance becomes excessive, the power loss of IGBT with larger current sharing increases, and there is a possibility of thermal destruction. Therefore, when selecting IGBTs to be connected in parallel, it is necessary to choose IGBTs with small $\Delta V_{CE(sat)}$. This concept applies to FWD as well.

1.1 Current imbalance caused by $\Delta V_{CE(sat)}$

Fig. 8-1 shows the output characteristics of two IGBTs (Q1 and Q2) with different $V_{CE(sat)}$. $\Delta V_{CE(sat)}$ is the $V_{CE(sat)}$ difference between Q1 and Q2. The output characteristics of Q_1 and Q_2 can be approximated by the following equations.

$$V_{CEQ1} = V_{01} + r_1 \cdot I_{C1}$$
$$r_1 = V_1/(I_{C1} - I_{C2})$$
$$V_{CEQ2} = V_{02} + r_2 \cdot I_{C2}$$
$$r_2 = V_2/(I_{C1} - I_{C2})$$

Based on the above, when collector current I_{Ctotal} (=I_{C1}+I_{C2}) flow through a circuit in which Q_1 and Q_2 are connected in parallel, the voltages across Q1 and Q2 being the same according to Kirchhoff's law, then each collector current can be calculated by the following equations, respectively.

$$I_{C1} = (V_{O2} - V_{O1} + r_2 \cdot I_{Ctotal})/(r_1 + r_2)$$
$$I_{C2} = (V_{O1} - V_{O2} + r_1 \cdot I_{Ctotal})/(r_1 + r_2)$$

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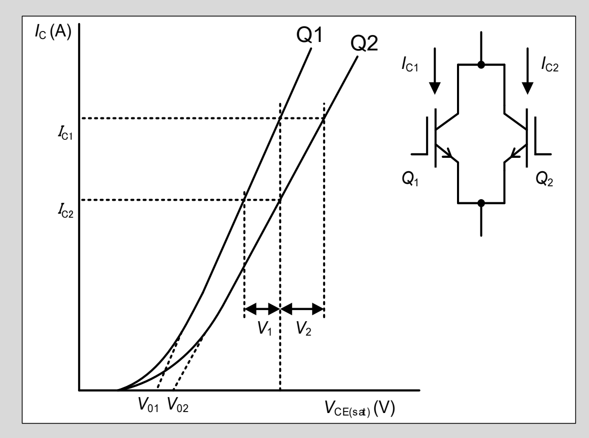

Fig. 8-1 Example of different output characteristics

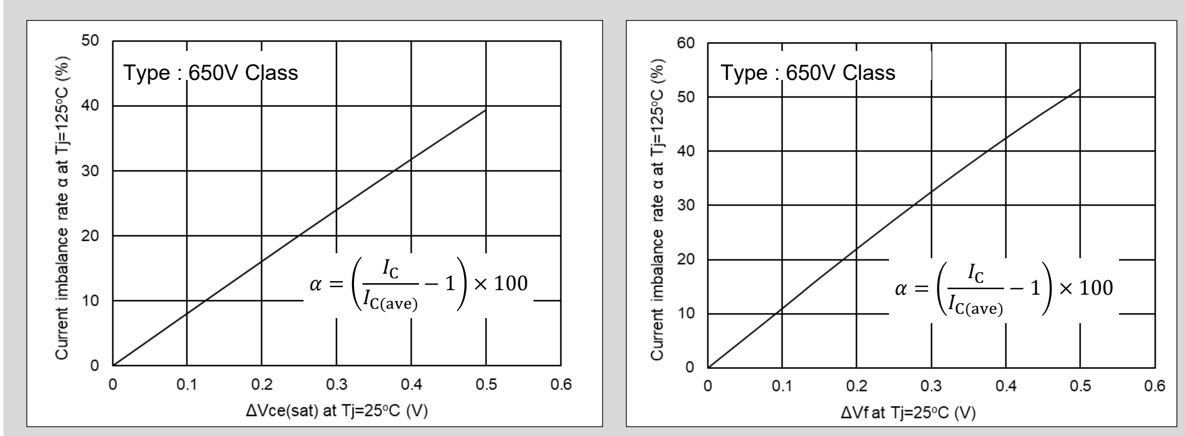

Fig. 8-2 ΔV and current imbalance ratio (left: IGBT, right: FWD)

In the above equations, if $V_{01}=V_{02}$, I_{C1} is r_2/r_1 times larger than I_{C2}. As shown in Fig. 8-1, since $r_2>r_1$, the current sharing of Q1, which is the IGBT with lower $V_{CE(sat)}$ becomes larger.

The ratio of current sharing is called the current imbalance ratio and is determined by $\Delta V_{CE(sat)}$ of each IGBT. Fig. 8-2 shows the relationship for two parallel connection of XS series discrete IGBTs. It can be seen that the current imbalance ratio increases as $\Delta V_{CE(sat)}$ increases. Therefore, when connecting IGBTs in parallel, it is important to combine products with small $\Delta V_{CE(sat)}$.

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1.2 $\Delta V_{CE(sat)}$ minimization

$\Delta V_{CE(sat)}$ can be minimized by using discrete IGBTs from the same product lot. This is because the influence of fabrication process, such as variations in raw materials, manufacturing, and inspection process can be minimized. Therefore, parallel connection with IGBTs from the same product lot is recommended.

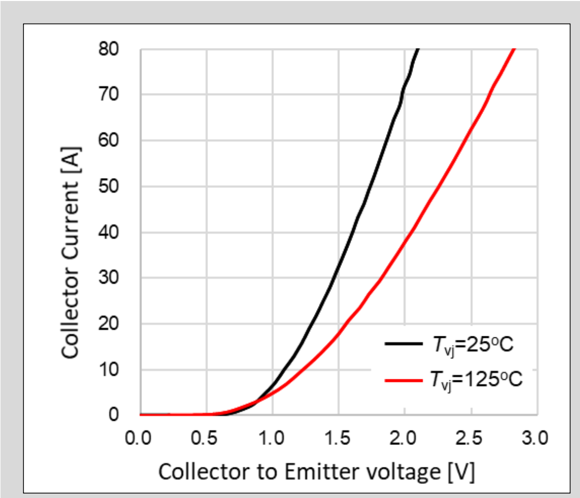
1.3 T_{vj} dependency of output characteristics and current imbalance

The output characteristics of both IGBTs and FWDs depend on the junction temperature (T_{vj}), and this dependency can affect the current imbalance when devices are connected in parallel. Therefore, it is important to consider T_{vj} effects when paralleling IGBTs or FWDs. As an example, Fig. 8-3 shows the output characteristics of a 40A rated XS series discrete IGBT and its FWD.

As described in section 1.1, when two IGBTs with $\Delta V_{CE(sat)}$ are connected in parallel, the IGBT with the lower $V_{CE(sat)}$ conducts more current. This higher current raises its conduction loss and thus its T_{vj} rises more than the other IGBT. Since the IGBT has a positive temperature coefficient, $V_{CE(sat)}$ increases as T_{vj} rises, and the current sharing decreases accordingly. In this way, in a combination of IGBTs with positive T_{vj} dependency, the current flowing through both IGBTs becomes balance due to temperature rise.

On the other hand, the FWD exhibits a negative temperature coefficient. When two FWDs with a ΔV_F are paralleled, the T_{vj} rise lowers the forward voltage V_F of the hotter device, causing it to conduct even more current and thus worsening the imbalance.

Therefore, when paralleling IGBTs or FWDs, increases in T_{vj} affects the current imbalance ratio. The current imbalance data shown in Fig. 8-2 already account for this temperature effect, which is why the imbalance ratio of FWD is larger than IGBT.



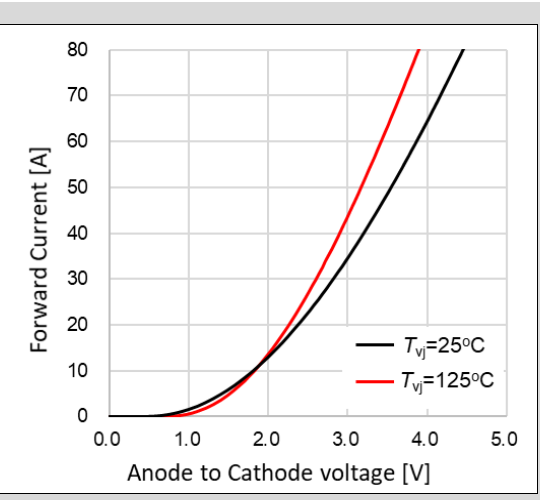


Fig. 8-3 Comparison of output characteristics (left: IGBT, right: FWD)

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1.4 Derating in parallel connection with multiple of IGBTs

When IGBTs are connected in parallel, the current imbalance must be taken into consideration, and the total current (maximum current that can flow) must be derated (decrease of total current) relative to the total rated current. When n-number of IGBTs are connected in parallel, the worst condition is current concentration in the IGBT with the lowest $V_{CE(sat)}$. Therefore, the allowable maximum current ΣI when n-number of IGBTs are connected in parallel can be expressed by the following formula, using the current imbalance rate α when two IGBTS are connected in parallel.

$$\sum I = I_{C(max)}\left[1+(n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right] \qquad \alpha = \left(\frac{I_{C1}}{I_{C(ave)}}-1\right)\cdot 100$$

Here, the current imbalance rate α in the above formula can be obtained from the current value I_{C1} and the average current value $I_{C(ave)}=(I_{C1}+I_{C2})/2$ for two parallel IGBTs as shown in Fig. 8-1. $I_{C(max)}$ is the maximum current for a single IGBT, and ΣI is the maximum current of the parallel connection. However, in order to operate with the maximum current ΣI, each IGBT connected in parallel must satisfy the RBSOA stated in the specification, and T_{vj} rise caused by power loss must be kept bellow $T_{vj(max)}$ as well. Note that T_{vj} rise varies depending on the operating conditions such as switching frequency, gate drive condition, cooling condition, snubber condition, etc.

The total current ΣI in a parallel connection requires derating with respect to the simple sum of currents ($n\cdot I_{C(max)}$). For example, if α=15%, $I_{C(max)}$=40A and n=4, then ΣI=128.7A. In this case, derating of 19.6% is required from the simple sum of 40x4=160A.

Fig. 8-4 shows the IGBT derating rate when α=15%. As shown in this figure, derating rate increases as the parallel number increases. Therefore, derate the total current according to the parallel number. Note that derating rate depends on the current imbalance rate.

The derating rate shown in this example is a reference value calculated from the current imbalance rate. Please determine the derating rate after verifying the imbalance rate by actual evaluation.

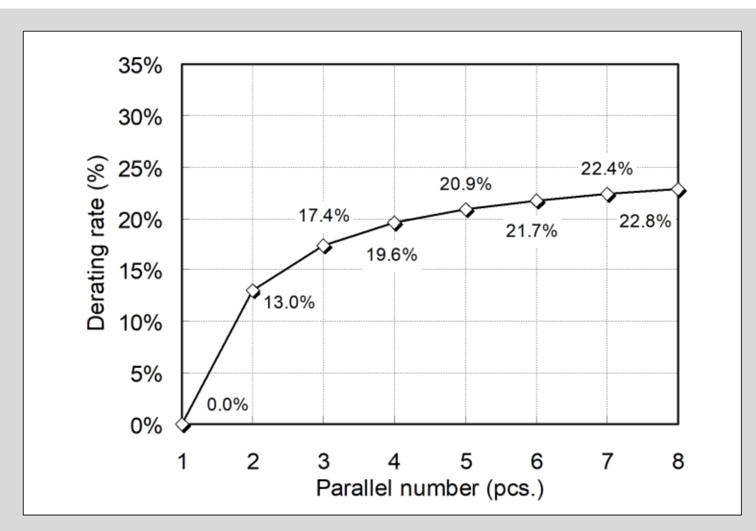

Fig. 8-4 Relationship between derating rate and parallel number

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2. Main Circuit Design

Variation in the main circuit wiring between each IGBT in a parallel connection has a large effect on the current imbalance during both steady-state operation and switching operation. Since this may lead to malfunction, it is necessary to keep the following two factors in mind and design the main circuit wiring symmetrically and as short as possible.

(1) Variation in main circuit wiring resistance

(2) Variation in main circuit wiring inductance

2.1 Variation in main circuit wiring resistance

Fig. 8-5 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring resistance. The collector side resistance component is omitted.

If the resistance component of the main circuit wiring is large, the total collector current flowing through Q1 and Q2 will decrease compared to when the resistance component is small. The larger the resistance component, the smaller the total collector current.

If the emitter side resistances are unequal (for example, $R_{E1} > R_{E2}$), then $I_{C1} < I_{C2}$, resulting in current imbalance between Q1 and Q2.

In this way, the resistance component of the main circuit may cause a decrease in collector current or current imbalance. To minimize these effects, the wiring on the emitter side must be as short and as symmetrical as possible.

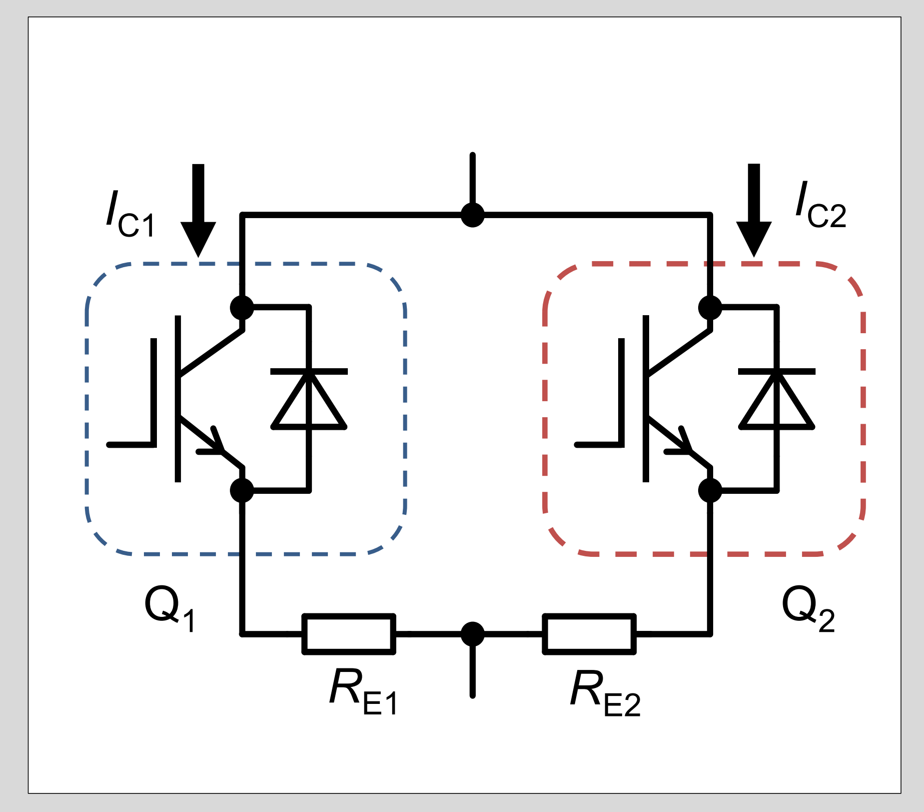

Fig. 8-5 Equivalent circuit of main circuit with wiring resistance component

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2.2 Variation in main circuit wiring inductance

Fig. 8-6 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring inductance. If the main circuit wiring inductance is uneven, current imbalance will occur between the IGBTs during switching. When collector currents I_{C1} and I_{C2} flow through IGBT Q1 and Q2, respectively, the current sharing is affected by the difference between the wiring inductances of each IGBT L_{E1} and L_{E2}. The current sharing is mostly determined by the inductance ratio. Therefore, in order to reduce the current imbalance during switching, it is necessary to design the wiring inductance as even as possible. If the wiring inductances L_{E1} and L_{E2} are different, there will be difference in the induced voltage of L_{E1} and L_{E2} caused by di/dt at turn-on. The difference in induced voltage affects the effective gate voltage of each IGBT and promotes current imbalance. For this reason, in a parallel connection, it is important to design the main circuit so that L_{E1}=L_{E2} as much as possible. Also, if the main circuit wiring inductance is large, the surge voltage at IGBT turn-off will increase. Therefore, it is necessary to design the wiring inductance as small as possible.

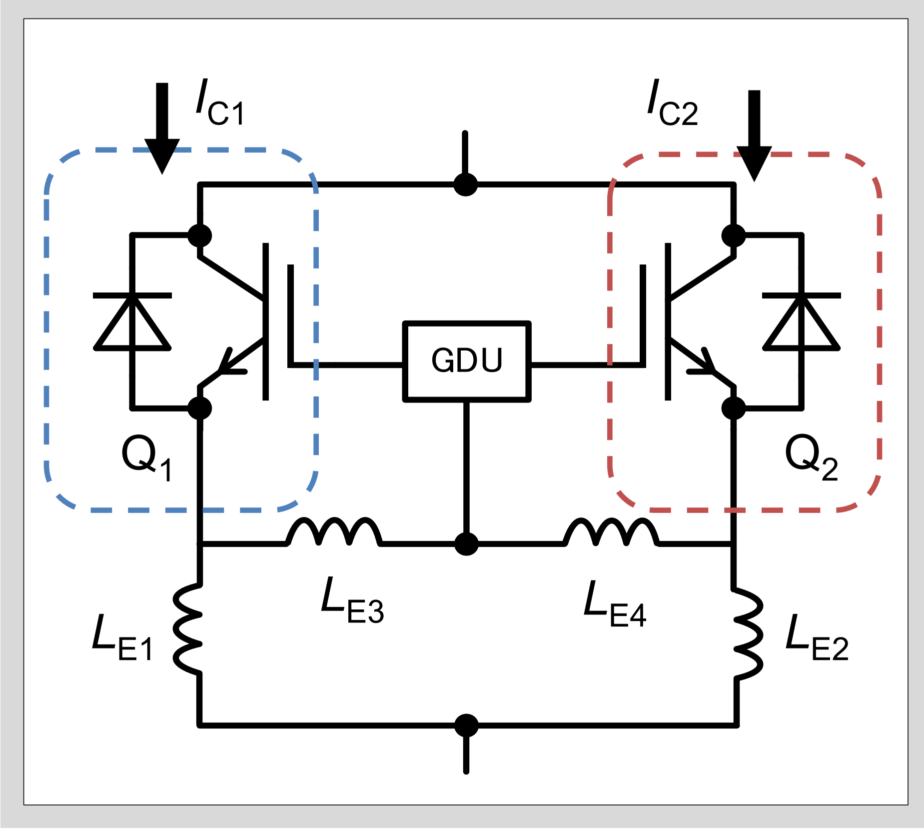

Fig. 8-6 Equivalent circuit of main circuit with wiring inductance component

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3. Gate Drive Circuit Design

In addition to the contents of Chapter 7, there are other precautions when designing gate drive circuits for parallel connection of discrete IGBTs. Also, there are different precautions depending on the gate driver configuration for parallel connection. If these precautions are not taken into consideration, the gate drive circuit may cause current imbalance or malfunction, possibly destroying the IGBTs. The main precautions when designing gate drive circuits for parallel connections are described as follows.

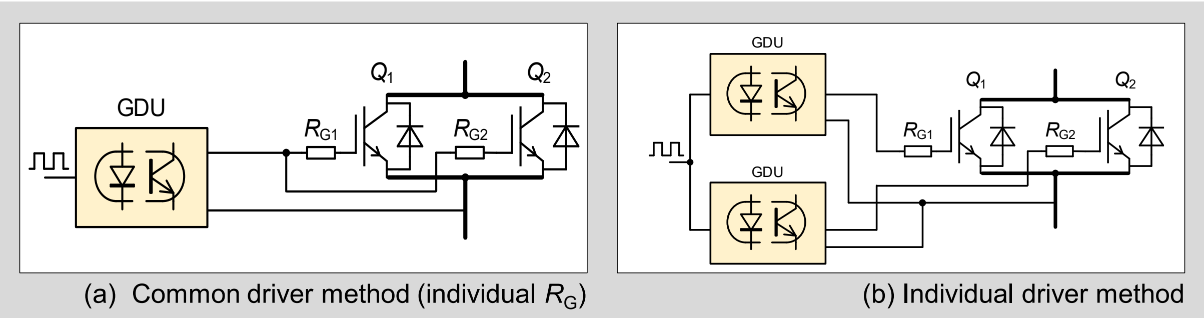
3.1 Connection of gate drive circuit to gate-emitter terminal

When driving parallel connected IGBTs, if the IGBT has auxiliary emitter terminal, use the auxiliary emitter terminal to drive the IGBT. If there is no auxiliary emitter terminal, and the emitter wiring of the gate drive circuit is connected at a position where the wiring inductances L_{E1} and L_{E2} as shown in Fig. 8-8 are uneven, the gate voltage of each IGBT during switching will differ, resulting in unbalanced transient current sharing. TO-247-4 packages have auxiliary emitter terminal for the gate drive circuit. Using this terminal will realize balanced L_{E1} and L_{E2}, thus transient current imbalance can be suppressed.

However, even if auxiliary emitter terminal is used to drive the IGBT, if the emitter wiring from the gate drive circuit to each IGBT is long and uneven, current imbalance will occur. Therefore, it is important to design the gate drive circuit wiring to each IGBT with equal length, as short as possible, and symmetrical. The gate drive circuit wiring should be twisted, and kept as far away from the main circuit wiring as possible and not parallel to each other.

3.2 Precautions when designing gate drive circuits for parallel connections

There are several gate drive circuit methods for parallel connection of discrete IGBTs, and precautions differ depending on the gate driver configuration. As an example of gate drive circuit configuration for parallel connection, Fig. 8-7(a) shows the common driver method (a configuration in which one gate driver drives all the IGBTs), and Fig. 8-7(b) shows the individual driver method (a configuration in which each IGBT is driven by individual gate drivers equal to the number of parallel IGBTs). Details of these two types of gate drive circuits and their design considerations are described in the following pages.



(a) Common driver method (individual R_G) (b) Individual driver method

Fig. 8-7 Gate drive circuit configuration for parallel connection

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3.2.1 Common driver method

A feature of the common driver method is that the power supply and optocoupler that drive each IGBT can be shared, thus the gate drive circuit can be simplified and the number of components can be reduced. On the other hand, driving multiple IGBTs connected in parallel with a single power supply requires a large power supply capacity.

In addition, the emitters of each parallel IGBT are common within the gate drive circuit, creating a closed loop which may generate gate voltage fluctuations during switching and cause the IGBTs to malfunction. The mechanism of the parasitic oscillation is shown in Fig. 8-8. If the wiring inductances L_{E1} and L_{E2} as shown in Fig. 8-6 are uneven, the difference in wiring inductance and the input capacitance of the IGBT will generate a cross current i_N, which will generate electromotive force in L_{E3} and L_{E4}, resulting in parasitic oscillation of the gate voltage.

As countermeasures, consider inserting a common mode choke in the gate circuit or a resistor R_E on the emitter side, and confirm that the problem described above does not occur.

Mechanism of parasitic oscillation during turn-on in common driver method

(a) When IGBTs Q1 and Q2 turns on, I_C increases and di/dt occurs in the main circuit. As a result, electromotive forces V_{LE1} and V_{LE2} are generated in the wiring inductances.

(b) When there is a difference in the wiring inductances, the magnitude of electromotive forces V_{LE1} and V_{LE2} will be different, generating a cross current i_N in the closed loop.

(c) Electromotive forces V_{LE3} and V_{LE4} are generated in the wiring inductances between the GDU and the emitter L_{E3} and L_{E4} by this cross current i_N, and parasitic oscillation of the gate voltage is generated by the charging and discharging currents to Q1 and Q2.

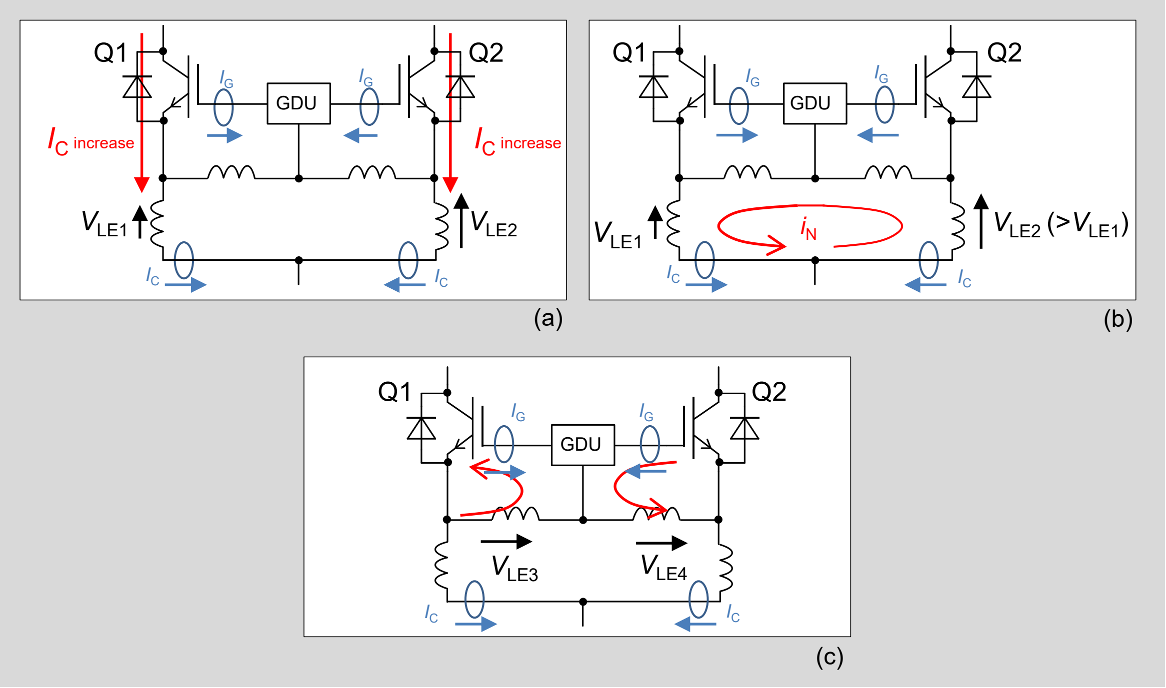

Fig. 8-8 Parasitic oscillation mechanism

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3.2.2 Individual driver method

A feature of the individual driver method is that the emitters of the parallel IGBTs are not common. In this case, a closed loop is not formed thus there will no cross current at the emitter, and risk of malfunction such as parasitic oscillation shown in Fig. 8-8 is reduced. On the other hand, arranging individual gate drive circuits for each parallel IGBT complicates the gate drive circuit. In addition, due to variations in the characteristics of electronic components such as optocouplers, each parallel IGBT has a difference in turn-on/turn-off timing, which may cause current imbalance or malfunction during switching. Therefore, when designing gate drive circuit for the individual driver method, it is necessary to minimize the difference in timing between turn-on and turn-off of each IGBT by considering the characteristics variation of electronic components.

3.2.3 Gate resistor configuration in common driver method

As shown in Fig. 8-9, there are three methods for configuring the gate resistor R_G in the common driver method.

In the case of the individual gate resistor method as shown in Fig. 8-9(a), the R_G connected to each IGBT can suppress the parasitic oscillation caused by the circuit inductance of the gate circuit wiring and the input capacitance of the IGBT. However, even if each IGBT is connected to the same driver IC, variations in the R_G can cause differences in the turn-on/turn-off timing of each IGBT during switching, which may cause current imbalance or malfunction.

In the case of the common gate resistor method as shown in Fig. 8-9(b), there will be no difference in the R_G value of each IGBT, so the difference in turn-on/turn-off timing of each IGBT can be minimized. However, due to LC resonance of the gate drive circuit wiring inductance and the input capacitance of the IGBT, parasitic oscillation may occur when the gate voltage rises.

If no parasitic oscillation or IGBT turn-on/turn-off timing difference is observed, it is possible to apply the common gate resistor method or the individual gate resistor method. However, when designing a new gate drive circuit, it is recommended to apply the combination gate resistor method as shown in Fig. 8-9(c), which combines the characteristics of both common gate resistor method and the individual gate resistor method.

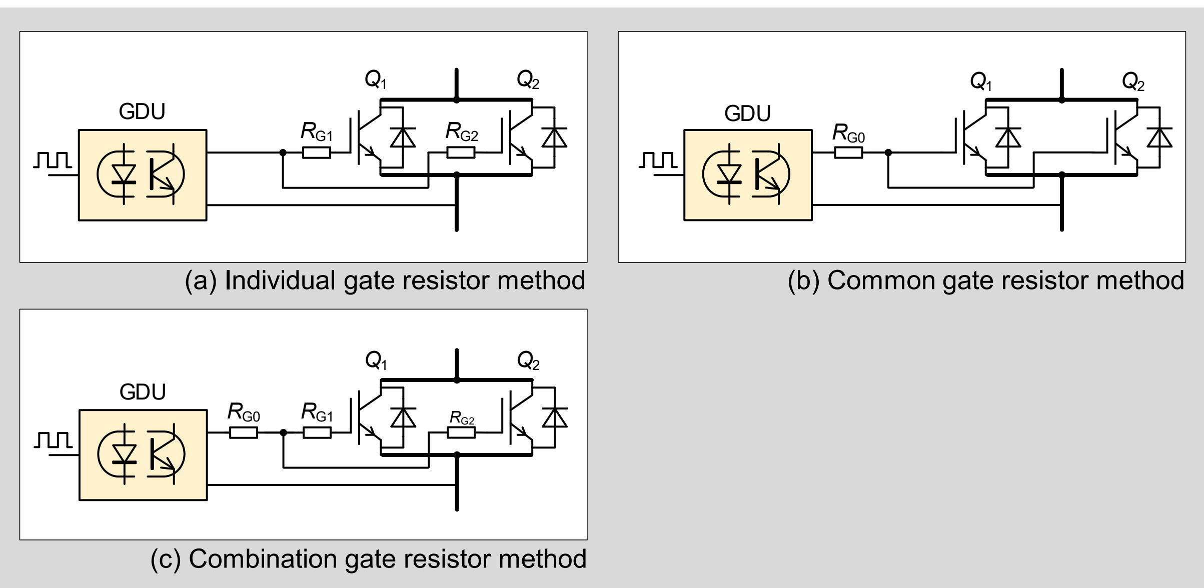

Fig. 8-9 Gate resistor configuration in common driver method

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4. Cooling Design

When connecting discrete IGBTs in parallel, it is necessary to consider the thermal interference of each IGBT. If the junction temperature T_{vj} increases due to thermal interference, the junction temperature absolute maximum rating $T_{vj(max)}$ may be exceeded and cause thermal destruction of the IGBTs. Therefore, it is necessary to consider the thermal interference between each IGBT and design the IGBTs layout to reduce T_{vj}. The points to consider regarding cooling design in parallel connection are shown below.

- Layout design considering thermal interference between each IGBT.
- Equalize cooling conditions for each IGBT.
- Uniform thermal grease thickness applied to each IGBT.

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Chapter 9 Evaluation and Measurement

1. Evaluation and Measurement Methods 9-2
2. Voltage Measurement 9-3
3. Current Measurement 9-5

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This chapter describes how to evaluate the characteristics of discrete IGBT, and the methods for measuring voltage and current.

1. Evaluation and Measurement Methods

During development of power electronics equipment, it is necessary to evaluate the characteristics and measure the load of the IGBT modules while they are installed in the equipment. An overview of the evaluation items and measurement methods is shown in Table 9-1.

Table 9-1 Overview of evaluation items and measurement methods

No.	Evaluation item	Measurement item	Measurement methods	Measuring instrument
1	Collector-Emitter voltage	Voltage	With G-E shorted, apply test voltage to C-E. *If there is possibility that the test voltage may exceed the rating of the components connected to C-E, disconnect those components first.	Curve tracer
2	Collector-Emitter saturation voltage		Measure by connecting a voltage clamping circuit between C-E so that the built-in amplifier of the oscilloscope does not saturate. *Static characteristics can be measured with a curve tracer or pulse h_{FE} meter	Oscilloscope
3	Turn-off surge voltage	Voltage	Measure the C-E voltage directly at the device terminals.	Oscilloscope
4	Switching time	Voltage Current	Measure the required voltage and current waveforms according to the switching time definition.	Oscilloscope
5	Current sharing (parallel connection)	Current	Measure the current flowing through each device.	Oscilloscope
6	Switching loss	Voltage Current	The product of the current and voltage is integrated over a specified period. (1) Calculate from voltage & current waveforms (2) Use a measuring instrument with math function	Oscilloscope
7	Operation locus		Plot the voltage & current during switching in current-voltage graph.	Oscilloscope
8	Case temperature	Temperature	Measure the temperature of the lead frame surface directly beneath the IGBT chip.	Thermocouple
9	Junction temperature		Create a calibration curve for the junction temperature and device characteristics with temperature dependence characteristics (for example, saturation voltage), and measure the characteristics of the device during operation to estimate the junction temperature.	-

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2. Voltage Measurement

Note that voltage measurement during IGBT operation is susceptible to noise caused by high-amplitude, high-speed switching operation.

2.1 Measuring instrument and calibration

Both the waveform and the target voltage value are important. Normally, an oscilloscope is used as the measuring instrument, and a voltage probe is used for voltage measurement. The time constant of the voltage divider RC of the probe/oscilloscope vary depending on the oscilloscope/probe combination. Therefore, before using the probe, carry out probe compensation to achieve uniform attenuation across all frequency range by connecting it to the calibration terminal of the oscilloscope.

Set the appropriate sensitivity (generally, 3 to 4 division amplitude on the display screen) and set the input coupling to DC. Exercise caution in selecting the probe, because the adjustment capacitance of the probe and the input capacitance of the oscilloscope must match to enable adjustment.

2.2 Saturation voltage measurement

Generally, while the circuit voltage using IGBT is as high as several hundred volts, the IGBT saturation voltage is as low as several volts. Because the size of the screen of the oscilloscope is limited, increasing the voltage sensitivity in an effort to measure the saturation voltage accurately will result in the display of a waveform that is different from the actual waveform due to effect such as saturation of the oscilloscope built-in amplifier. Therefore, the IGBT saturation voltage during switching operation cannot be measured by directly measuring the C-E voltage of the IGBT with an oscilloscope. The method to measure the saturation voltage is by adding a voltage clipping circuit as shown in Fig. 9-1, and measure $V_{CE(sat)}$ through that circuit.

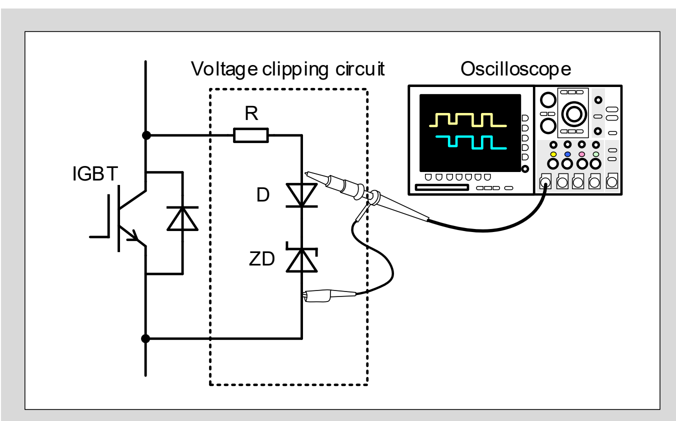

Fig. 9-1 Measurement method of saturation voltage

In Fig. 9-1, the Zener diode (ZD) limits the high voltage when the IGBT is turned off. Generally, a Zener diode with Zener voltage of 10V or less is used. R is a current-limiting resistor. Because most of the circuit voltage is applied to this resistor when the IGBT is turned off, the resistor must have a relatively large capacity. The diode (D) prevents the charges built in the junction capacitance of the Zener diode from discharging, and also prevents a RC filter from being formed by the junction capacitance and the current-limiting resistance.

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2.3 Surge voltage measurement (Collector-emitter voltage measurement)

While IGBTs offer the benefit of fast switching, the current change rate (-d*i*/d*t*) at turn-off is large, inducing a high voltage in the main circuit wiring inductance (L_S) of the equipment. This voltage is superimposed over the DC circuit voltage and cause a spike voltage to be applied to the device. This voltage is called surge voltage, and it is necessary to confirm that the voltage is within a predetermined voltage margin with respect to the maximum rating of the device.

The surge voltage can be measured at the device terminals with an oscilloscope and directly reading the value on the oscilloscope screen. Note the following precautions during measurement.

- Use a probe and an oscilloscope with sufficient frequency bandwidth.
- Adjust the oscilloscope sensitivity and calibrate the probe.
- Connect the measurement probe directly to the device terminals.

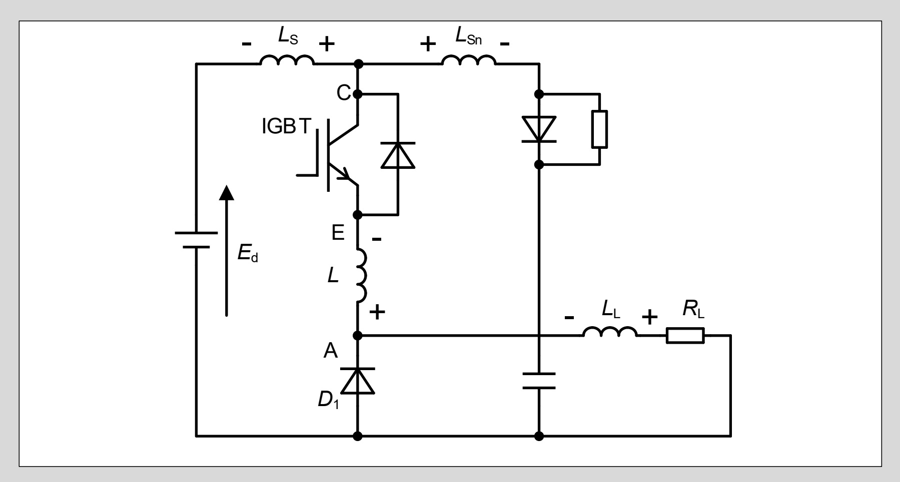

Fig. 9-2 Example of surge voltage measurement circuit

During IGBT turn-off, voltages of the polarity shown in Fig. 9-2 are induced in the circuit inductances of each part of the circuit. Note that in the case where V_{CA} is measured instead of V_{CE}, then a voltage lower than V_{CE} by $-L \cdot di/dt$ will be erroneously measured. Therefore, when measuring the surge voltage of the IGBT, it is necessary to measure it in a state where the influence of the wiring inductance L is minimized, such as by connecting the voltage probe directly to the module terminal.

- Keep the probe measurement leads as short as possible.
- Keep probe leads away from high d*i*/d*t* areas so that noise interferences are minimized.

When the voltage probe is connected to the switching circuit, the reference potential of the oscilloscope would equal the switching circuit. If there is a large ground potential fluctuation in the switching circuit, common-mode current would flow through the power line of the oscilloscope, which may cause the internal circuit to malfunction. Noise interferences can be verified by the following methods.

- Consider whether the measured waveform can be logically explained.
- Comparing with waveforms measured on a battery-powered oscilloscope that is less susceptible to noise interferences.

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2.4 Gate voltage measurement (Gate-emitter voltage measurement)

The V_{GE} can be directly measured with an oscilloscope similar to the surge voltage. However, since the IGBT gate is a capacitive load and the voltage probe also has capacitive impedance, do not attach or detach the voltage probe during measurement. The same precautions as for the surge voltage measurement are required.

3. Current Measurement

Current probes are used for current measurement. However, in practical equipment, the main circuit is compact in order to reduce wiring inductances L_S and simplify the structure. Thus, the wiring needs to be extended to measure the device current. A current transformer can be used to minimize the wiring extension. In addition, the use of current transformers is also necessary due to the limited measuring capacity of the current probe.

Current probe can measure current while maintaining insulation from the conductive part, but in addition to being an electromagnetic induction-based detector, the signal level is low that it is susceptible to induction caused noise interferences. Care should be taken against noise interferences.

3.1 Current probe sensitivity check

Before making any measurements, it is necessary to check the probe sensitivity.

Current probe can be calibrated using the oscilloscope calibrator output or using an oscillator as shown in Fig. 9-3. The measurement method in Fig. 9-3 uses a known resistance *R* (non-inductive) to measure the voltage *e* across *R* to obtain the current *i*. Compare the current *i* and the waveform of the current probe to calibrate. If the current *i* is too small, sensitivity can be increased by increasing the number of primary winding of the current probe.

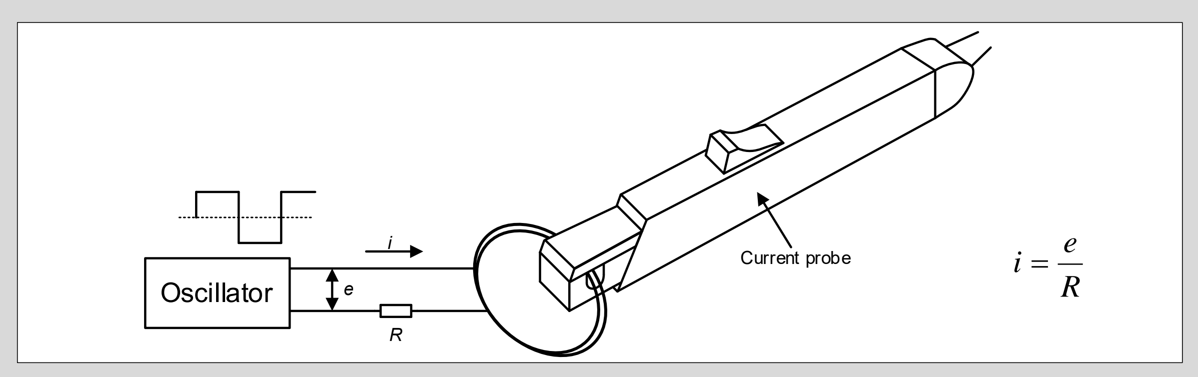

Fig. 9-3 Current probe calibration method

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3.2 Current measurement method

Using a two parallel connection as example, Fig. 9-4 shows where current transformers (CT) are inserted to measure the current. When measuring the current on the positive side of T_{11}, measure the secondary side current of CT_1 with a current probe. For T_{12}, measure the secondary side current. The total current on the positive side (sum of T_{11} current and T_{12} current) can be measured with the same current probe by aligning the directions of the secondary side currents of CT_1 and CT_2 and measuring them at once.

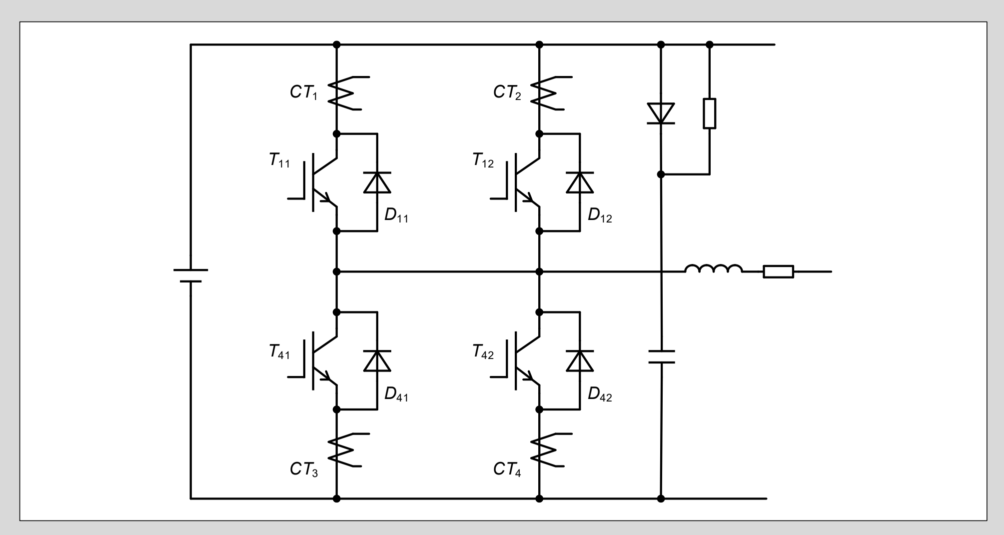

Fig. 9-4 CT insert position and current measurement method

3.3 Switching loss measurement

Switching loss is the loss generated during the period from the start of switching to the end of switching operation and reaching a steady-state. For example, the turn-on loss is the loss that is generated from V_{GE} is above 0V until V_{CE} reaches the saturation voltage.

The switching loss is generally expressed in terms of energy generated per instance of switching.

Fig. 9-5 shows example of switching waveform and switching loss. To measure switching loss, the current and voltage waveforms must be measured correctly. Note that when current and voltage are measured simultaneously, the common-mode current flowing from the voltage probe may cause the current waveform to be distorted. The presence or absence of this common-mode effect can be determined by comparing the current waveforms before and after the voltage probe is connected. If the current waveform is distorted, inserting a common-mode choke into the voltage probe cable and the oscilloscope power cable (by winding the cable around a core with excellent high frequency characteristics) as shown in Fig. 9-6 will reduce the waveform distortion.

In addition, the settings of reference 0V and 0A is important. Note that when using an AC current probe, the position of 0A varies depending on the current value and the conduction ratio.

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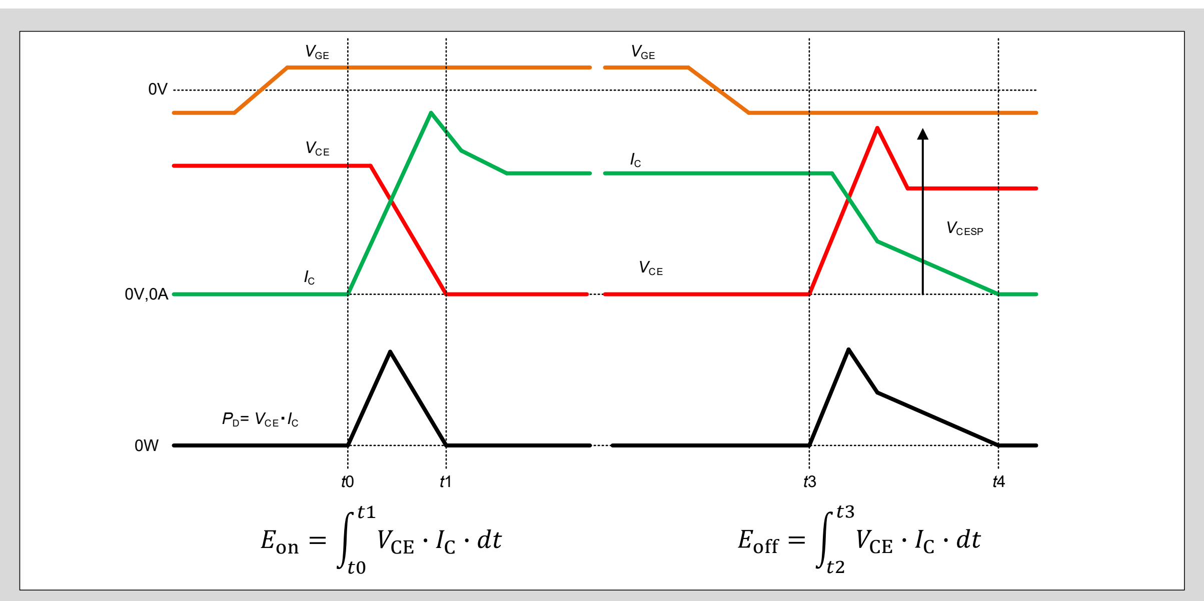

Fig. 9-5 Switching loss

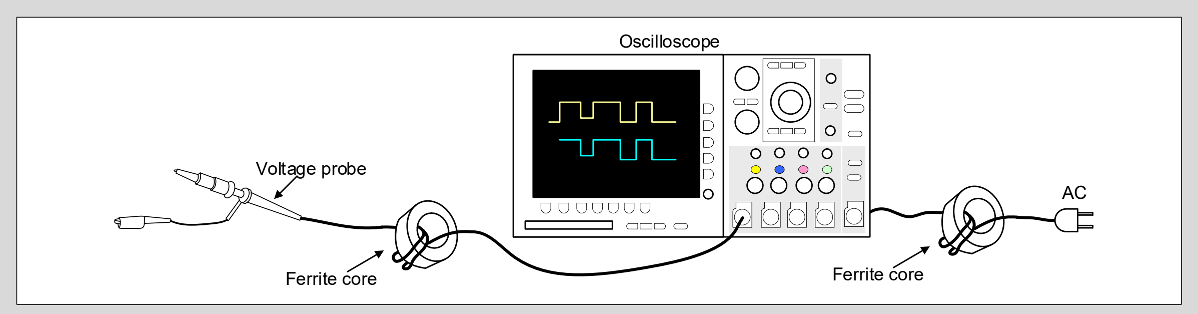

Fig. 9-6 Inserting common mode choke

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