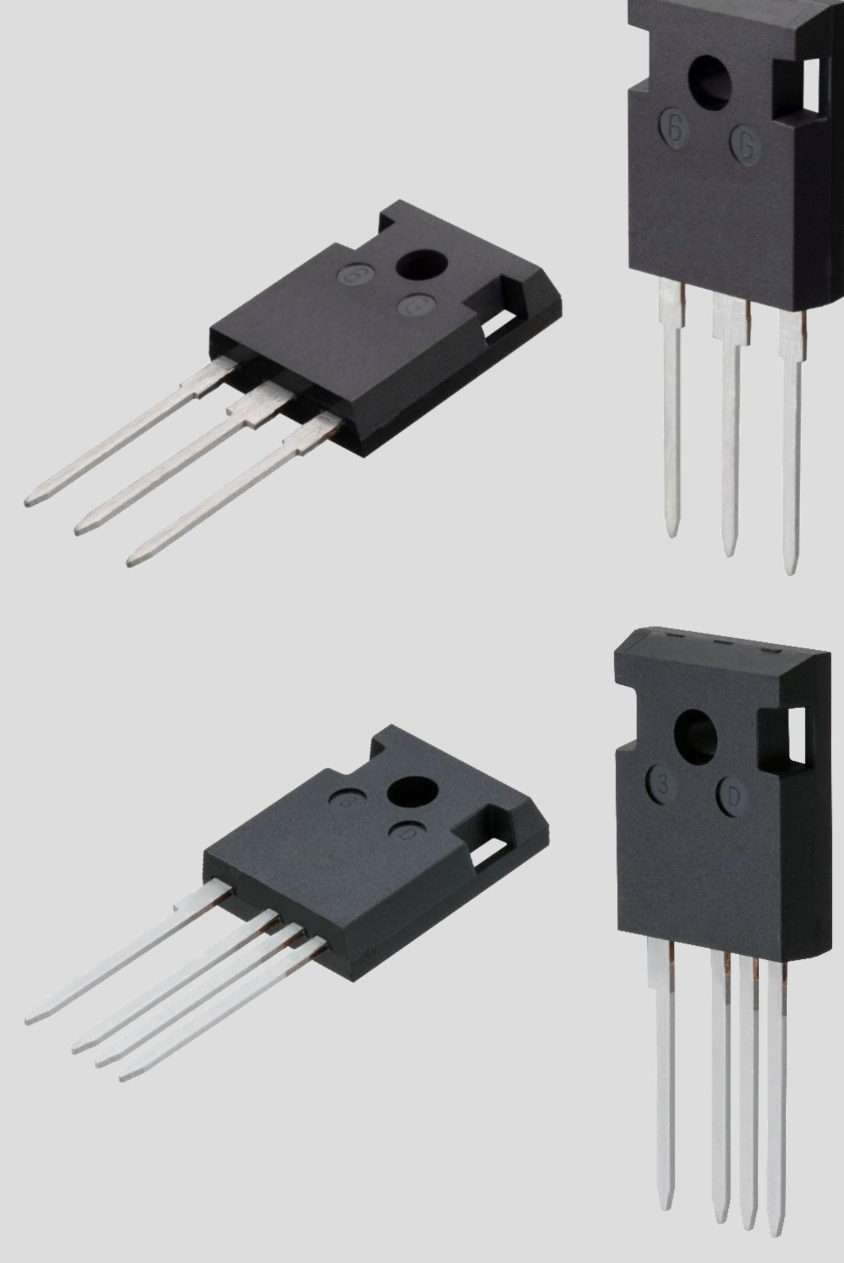

Discrete IGBT

Application Manual

Dec. 2025

Fuji Electric Co., Ltd.

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⚠Cautions

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Chapter 8 Parallel Connections

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The IGBT current capacity can be increased by connecting discrete IGBTs in parallel. However, in this case, it is necessary to consider the current imbalance between the IGBTs, the temperature distribution, and the increase in noise and surge voltage due to the increase in wiring length.

Note the following points when connecting IGBTs in parallel.

1. Selection of IGBT
2. Main circuit design
3. Gate drive circuit design
4. Cooling design

This chapter describes the details of each point when connecting IGBTs in parallel.

1. Selection of Discrete IGBTs

Points to consider when connecting IGBTs in parallel are $V_{CE(sat)}$ variation ($\Delta V_{CE(sat)}$) and temperature dependent characteristic differences among the IGBTs on the same arm. Due to this $\Delta V_{CE(sat)}$, that is, the difference in the output characteristics of each IGBT, current imbalance occurs in the steady-state. If this current imbalance becomes excessive, the power loss of IGBT with larger current sharing increases, and there is a possibility of thermal destruction. Therefore, when selecting IGBTs to be connected in parallel, it is necessary to choose IGBTs with small $\Delta V_{CE(sat)}$. This concept applies to FWD as well.

1.1 Current imbalance caused by $\Delta V_{CE(sat)}$

Fig. 8-1 shows the output characteristics of two IGBTs (Q1 and Q2) with different $V_{CE(sat)}$. $\Delta V_{CE(sat)}$ is the $V_{CE(sat)}$ difference between Q1 and Q2. The output characteristics of Q_1 and Q_2 can be approximated by the following equations.

$$V_{CEQ1} = V_{01} + r_1 \cdot I_{C1}$$
$$r_1 = V_1/(I_{C1} - I_{C2})$$
$$V_{CEQ2} = V_{02} + r_2 \cdot I_{C2}$$
$$r_2 = V_2/(I_{C1} - I_{C2})$$

Based on the above, when collector current I_{Ctotal} ($=I_{C1}+I_{C2}$) flow through a circuit in which Q_1 and Q_2 are connected in parallel, the voltages across Q1 and Q2 being the same according to Kirchhoff's law, then each collector current can be calculated by the following equations, respectively.

$$I_{C1} = (V_{O2} - V_{O1} + r_2 \cdot I_{Ctotal})/(r_1 + r_2)$$
$$I_{C2} = (V_{O1} - V_{O2} + r_1 \cdot I_{Ctotal})/(r_1 + r_2)$$

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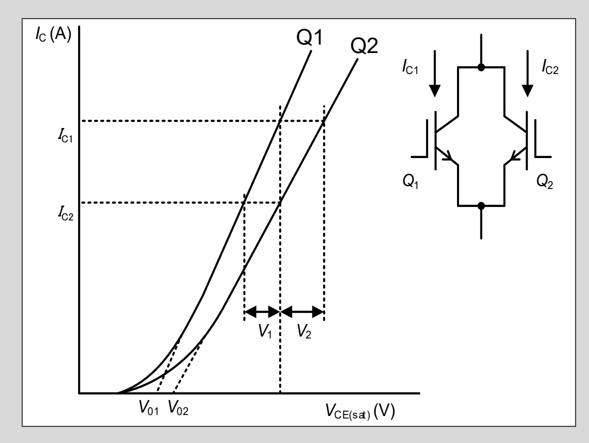

Fig. 8-1 Example of different output characteristics

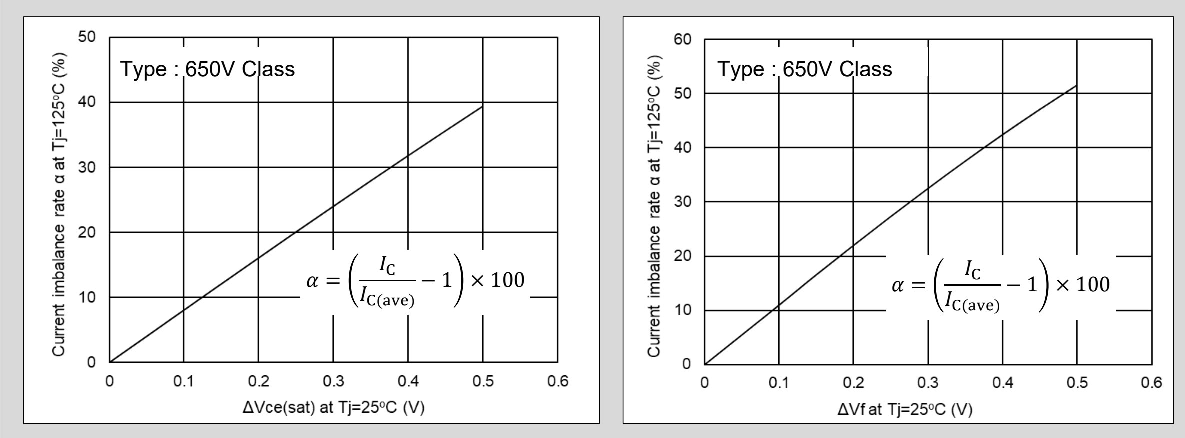

Fig. 8-2 Δ*V* and current imbalance ratio (left: IGBT, right: FWD)

In the above equations, if $V_{01}=V_{02}$, I_{C1} is r_2/r_1 times larger than I_{C2}. As shown in Fig. 8-1, since $r_2>r_1$, the current sharing of Q1, which is the IGBT with lower $V_{CE(sat)}$ becomes larger.

The ratio of current sharing is called the current imbalance ratio and is determined by $\Delta V_{CE(sat)}$ of each IGBT. Fig. 8-2 shows the relationship for two parallel connection of XS series discrete IGBTs. It can be seen that the current imbalance ratio increases as $\Delta V_{CE(sat)}$ increases. Therefore, when connecting IGBTs in parallel, it is important to combine products with small $\Delta V_{CE(sat)}$.

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1.2 $\Delta V_{CE(sat)}$ minimization

$\Delta V_{CE(sat)}$ can be minimized by using discrete IGBTs from the same product lot. This is because the influence of fabrication process, such as variations in raw materials, manufacturing, and inspection process can be minimized. Therefore, parallel connection with IGBTs from the same product lot is recommended.

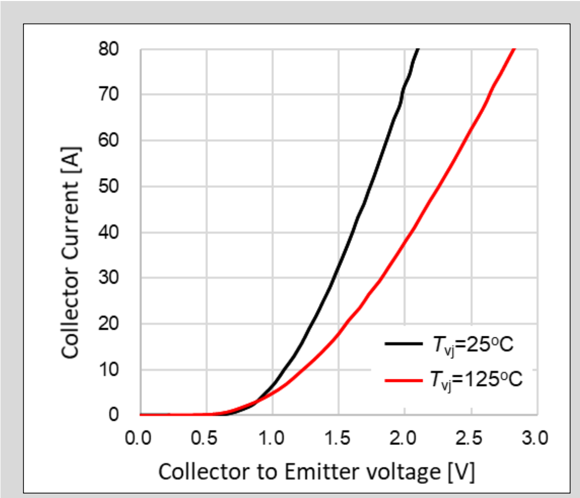
1.3 T_{vj} dependency of output characteristics and current imbalance

The output characteristics of both IGBTs and FWDs depend on the junction temperature (T_{vj}), and this dependency can affect the current imbalance when devices are connected in parallel. Therefore, it is important to consider T_{vj} effects when paralleling IGBTs or FWDs. As an example, Fig. 8-3 shows the output characteristics of a 40A rated XS series discrete IGBT and its FWD.

As described in section 1.1, when two IGBTs with $\Delta V_{CE(sat)}$ are connected in parallel, the IGBT with the lower $V_{CE(sat)}$ conducts more current. This higher current raises its conduction loss and thus its T_{vj} rises more than the other IGBT. Since the IGBT has a positive temperature coefficient, $V_{CE(sat)}$ increases as T_{vj} rises, and the current sharing decreases accordingly. In this way, in a combination of IGBTs with positive T_{vj} dependency, the current flowing through both IGBTs becomes balance due to temperature rise.

On the other hand, the FWD exhibits a negative temperature coefficient. When two FWDs with a ΔV_F are paralleled, the T_{vj} rise lowers the forward voltage V_F of the hotter device, causing it to conduct even more current and thus worsening the imbalance.

Therefore, when paralleling IGBTs or FWDs, increases in T_{vj} affects the current imbalance ratio. The current imbalance data shown in Fig. 8-2 already account for this temperature effect, which is why the imbalance ratio of FWD is larger than IGBT.



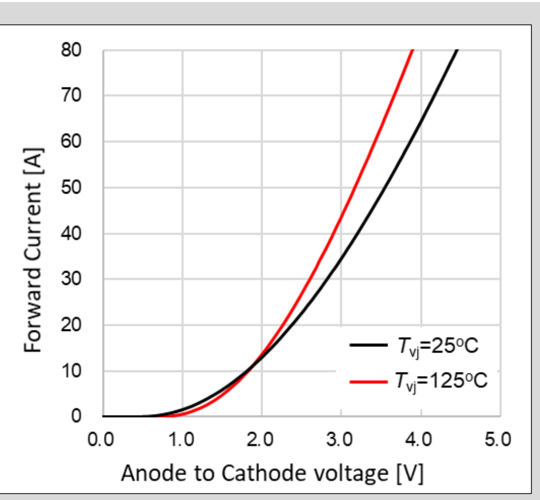


Fig. 8-3 Comparison of output characteristics (left: IGBT, right: FWD)

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1.4 Derating in parallel connection with multiple of IGBTs

When IGBTs are connected in parallel, the current imbalance must be taken into consideration, and the total current (maximum current that can flow) must be derated (decrease of total current) relative to the total rated current. When n-number of IGBTs are connected in parallel, the worst condition is current concentration in the IGBT with the lowest $V_{CE(sat)}$. Therefore, the allowable maximum current ΣI when n-number of IGBTs are connected in parallel can be expressed by the following formula, using the current imbalance rate α when two IGBTS are connected in parallel.

$$\sum I = I_{C(max)}\left[1 + (n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right] \qquad \alpha = \left(\frac{I_{C1}}{I_{C(ave)}} - 1\right)\cdot 100$$

Here, the current imbalance rate α in the above formula can be obtained from the current value I_{C1} and the average current value $I_{C(ave)}=(I_{C1}+I_{C2})/2$ for two parallel IGBTs as shown in Fig. 8-1. $I_{C(max)}$ is the maximum current for a single IGBT, and ΣI is the maximum current of the parallel connection. However, in order to operate with the maximum current ΣI, each IGBT connected in parallel must satisfy the RBSOA stated in the specification, and T_{vj} rise caused by power loss must be kept bellow $T_{vj(max)}$ as well. Note that T_{vj} rise varies depending on the operating conditions such as switching frequency, gate drive condition, cooling condition, snubber condition, etc.

The total current ΣI in a parallel connection requires derating with respect to the simple sum of currents ($n\cdot I_{C(max)}$). For example, if α=15%, $I_{C(max)}$=40A and n=4, then ΣI=128.7A. In this case, derating of 19.6% is required from the simple sum of 40x4=160A.

Fig. 8-4 shows the IGBT derating rate when α=15%. As shown in this figure, derating rate increases as the parallel number increases. Therefore, derate the total current according to the parallel number. Note that derating rate depends on the current imbalance rate.

The derating rate shown in this example is a reference value calculated from the current imbalance rate. Please determine the derating rate after verifying the imbalance rate by actual evaluation.

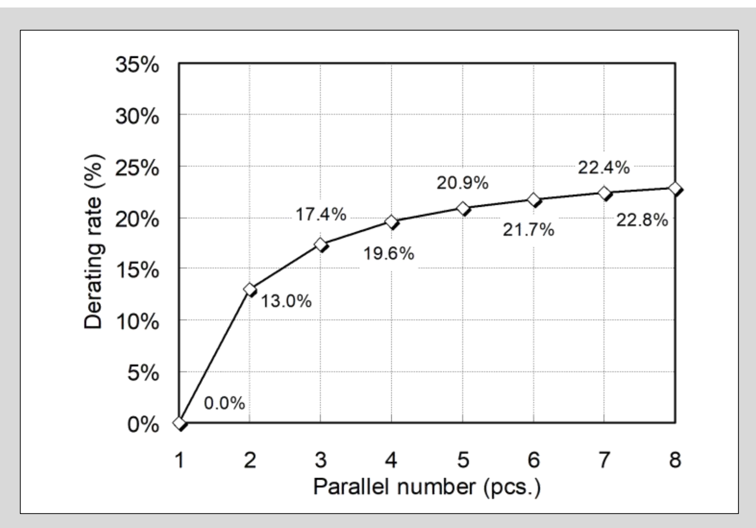

Fig. 8-4 Relationship between derating rate and parallel number

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2. Main Circuit Design

Variation in the main circuit wiring between each IGBT in a parallel connection has a large effect on the current imbalance during both steady-state operation and switching operation. Since this may lead to malfunction, it is necessary to keep the following two factors in mind and design the main circuit wiring symmetrically and as short as possible.

(1) Variation in main circuit wiring resistance
(2) Variation in main circuit wiring inductance

2.1 Variation in main circuit wiring resistance

Fig. 8-5 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring resistance. The collector side resistance component is omitted.

If the resistance component of the main circuit wiring is large, the total collector current flowing through Q1 and Q2 will decrease compared to when the resistance component is small. The larger the resistance component, the smaller the total collector current.

If the emitter side resistances are unequal (for example, $R_{E1} > R_{E2}$), then $I_{C1} < I_{C2}$, resulting in current imbalance between Q1 and Q2.

In this way, the resistance component of the main circuit may cause a decrease in collector current or current imbalance. To minimize these effects, the wiring on the emitter side must be as short and as symmetrical as possible.

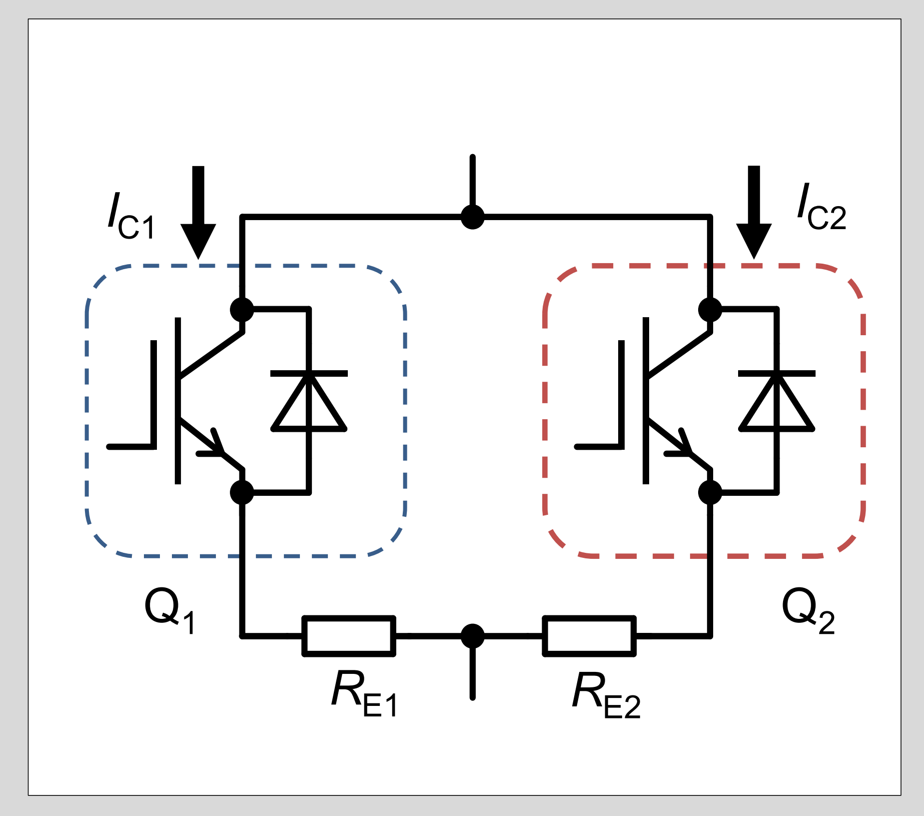

Fig. 8-5 Equivalent circuit of main circuit with wiring resistance component

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2.2 Variation in main circuit wiring inductance

Fig. 8-6 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring inductance. If the main circuit wiring inductance is uneven, current imbalance will occur between the IGBTs during switching. When collector currents I_{C1} and I_{C2} flow through IGBT Q1 and Q2, respectively, the current sharing is affected by the difference between the wiring inductances of each IGBT L_{E1} and L_{E2}. The current sharing is mostly determined by the inductance ratio. Therefore, in order to reduce the current imbalance during switching, it is necessary to design the wiring inductance as even as possible. If the wiring inductances L_{E1} and L_{E2} are different, there will be difference in the induced voltage of L_{E1} and L_{E2} caused by di/dt at turn-on. The difference in induced voltage affects the effective gate voltage of each IGBT and promotes current imbalance. For this reason, in a parallel connection, it is important to design the main circuit so that L_{E1}=L_{E2} as much as possible. Also, if the main circuit wiring inductance is large, the surge voltage at IGBT turn-off will increase. Therefore, it is necessary to design the wiring inductance as small as possible.

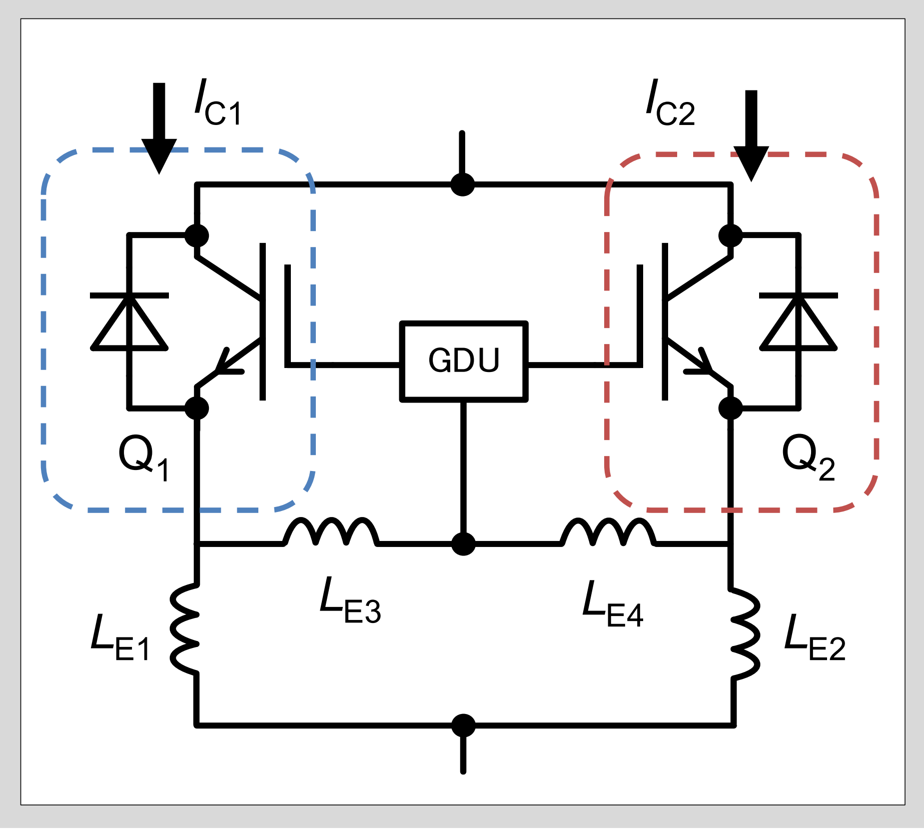

Fig. 8-6 Equivalent circuit of main circuit with wiring inductance component

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3. Gate Drive Circuit Design

In addition to the contents of Chapter 7, there are other precautions when designing gate drive circuits for parallel connection of discrete IGBTs. Also, there are different precautions depending on the gate driver configuration for parallel connection. If these precautions are not taken into consideration, the gate drive circuit may cause current imbalance or malfunction, possibly destroying the IGBTs. The main precautions when designing gate drive circuits for parallel connections are described as follows.

3.1 Connection of gate drive circuit to gate-emitter terminal

When driving parallel connected IGBTs, if the IGBT has auxiliary emitter terminal, use the auxiliary emitter terminal to drive the IGBT. If there is no auxiliary emitter terminal, and the emitter wiring of the gate drive circuit is connected at a position where the wiring inductances L_{E1} and L_{E2} as shown in Fig. 8-8 are uneven, the gate voltage of each IGBT during switching will differ, resulting in unbalanced transient current sharing. TO-247-4 packages have auxiliary emitter terminal for the gate drive circuit. Using this terminal will realize balanced L_{E1} and L_{E2}, thus transient current imbalance can be suppressed.

However, even if auxiliary emitter terminal is used to drive the IGBT, if the emitter wiring from the gate drive circuit to each IGBT is long and uneven, current imbalance will occur. Therefore, it is important to design the gate drive circuit wiring to each IGBT with equal length, as short as possible, and symmetrical. The gate drive circuit wiring should be twisted, and kept as far away from the main circuit wiring as possible and not parallel to each other.

3.2 Precautions when designing gate drive circuits for parallel connections

There are several gate drive circuit methods for parallel connection of discrete IGBTs, and precautions differ depending on the gate driver configuration. As an example of gate drive circuit configuration for parallel connection, Fig. 8-7(a) shows the common driver method (a configuration in which one gate driver drives all the IGBTs), and Fig. 8-7(b) shows the individual driver method (a configuration in which each IGBT is driven by individual gate drivers equal to the number of parallel IGBTs). Details of these two types of gate drive circuits and their design considerations are described in the following pages.

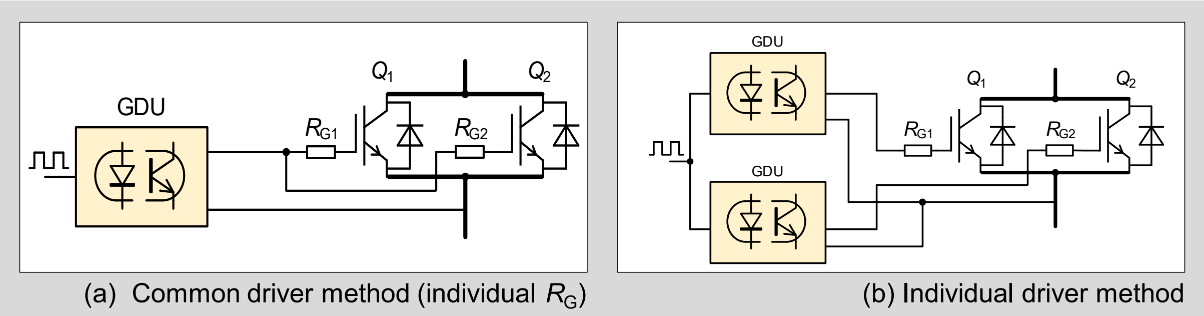

Fig. 8-7 Gate drive circuit configuration for parallel connection

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3.2.1 Common driver method

A feature of the common driver method is that the power supply and optocoupler that drive each IGBT can be shared, thus the gate drive circuit can be simplified and the number of components can be reduced. On the other hand, driving multiple IGBTs connected in parallel with a single power supply requires a large power supply capacity.

In addition, the emitters of each parallel IGBT are common within the gate drive circuit, creating a closed loop which may generate gate voltage fluctuations during switching and cause the IGBTs to malfunction. The mechanism of the parasitic oscillation is shown in Fig. 8-8. If the wiring inductances L_{E1} and L_{E2} as shown in Fig. 8-6 are uneven, the difference in wiring inductance and the input capacitance of the IGBT will generate a cross current i_N, which will generate electromotive force in L_{E3} and L_{E4}, resulting in parasitic oscillation of the gate voltage.

As countermeasures, consider inserting a common mode choke in the gate circuit or a resistor R_E on the emitter side, and confirm that the problem described above does not occur.

<u>Mechanism of parasitic oscillation during turn-on in common driver method</u>

(a) When IGBTs Q1 and Q2 turns on, I_C increases and di/dt occurs in the main circuit. As a result, electromotive forces V_{LE1} and V_{LE2} are generated in the wiring inductances.

(b) When there is a difference in the wiring inductances, the magnitude of electromotive forces V_{LE1} and V_{LE2} will be different, generating a cross current i_N in the closed loop.

(c) Electromotive forces V_{LE3} and V_{LE4} are generated in the wiring inductances between the GDU and the emitter L_{E3} and L_{E4} by this cross current i_N, and parasitic oscillation of the gate voltage is generated by the charging and discharging currents to Q1 and Q2.

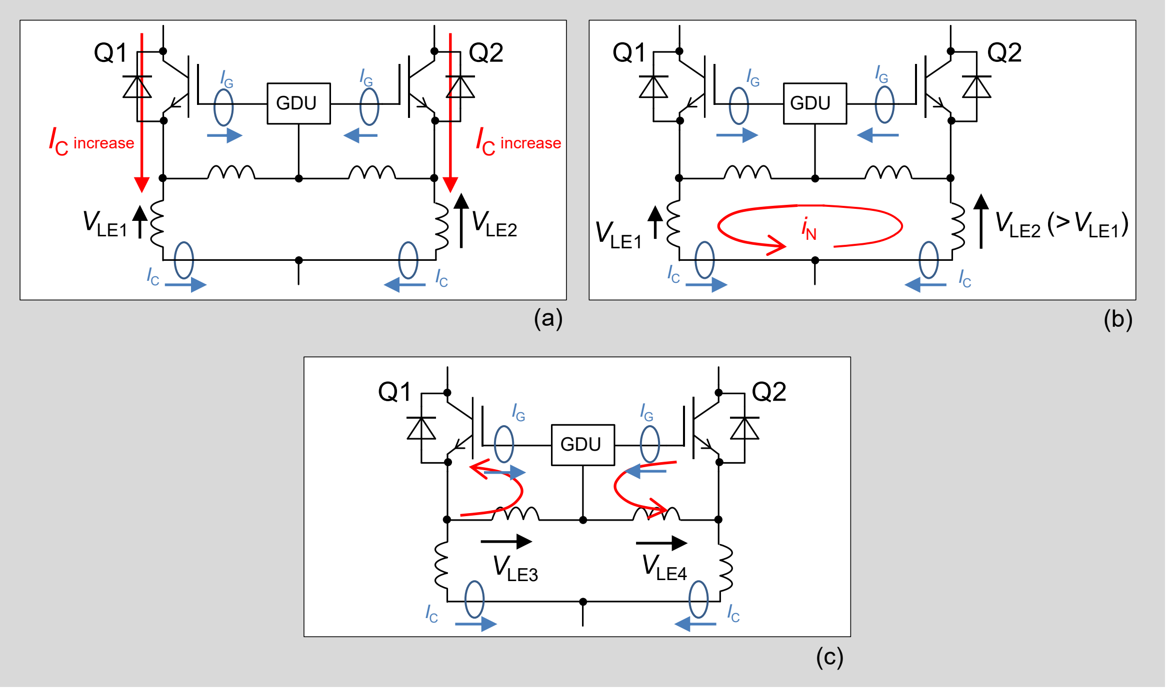

Fig. 8-8 Parasitic oscillation mechanism

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3.2.2 Individual driver method

A feature of the individual driver method is that the emitters of the parallel IGBTs are not common. In this case, a closed loop is not formed thus there will no cross current at the emitter, and risk of malfunction such as parasitic oscillation shown in Fig. 8-8 is reduced. On the other hand, arranging individual gate drive circuits for each parallel IGBT complicates the gate drive circuit. In addition, due to variations in the characteristics of electronic components such as optocouplers, each parallel IGBT has a difference in turn-on/turn-off timing, which may cause current imbalance or malfunction during switching. Therefore, when designing gate drive circuit for the individual driver method, it is necessary to minimize the difference in timing between turn-on and turn-off of each IGBT by considering the characteristics variation of electronic components.

3.2.3 Gate resistor configuration in common driver method

As shown in Fig. 8-9, there are three methods for configuring the gate resistor R_G in the common driver method.

In the case of the individual gate resistor method as shown in Fig. 8-9(a), the R_G connected to each IGBT can suppress the parasitic oscillation caused by the circuit inductance of the gate circuit wiring and the input capacitance of the IGBT. However, even if each IGBT is connected to the same driver IC, variations in the R_G can cause differences in the turn-on/turn-off timing of each IGBT during switching, which may cause current imbalance or malfunction.

In the case of the common gate resistor method as shown in Fig. 8-9(b), there will be no difference in the R_G value of each IGBT, so the difference in turn-on/turn-off timing of each IGBT can be minimized. However, due to LC resonance of the gate drive circuit wiring inductance and the input capacitance of the IGBT, parasitic oscillation may occur when the gate voltage rises.

If no parasitic oscillation or IGBT turn-on/turn-off timing difference is observed, it is possible to apply the common gate resistor method or the individual gate resistor method. However, when designing a new gate drive circuit, it is recommended to apply the combination gate resistor method as shown in Fig. 8-9(c), which combines the characteristics of both common gate resistor method and the individual gate resistor method.

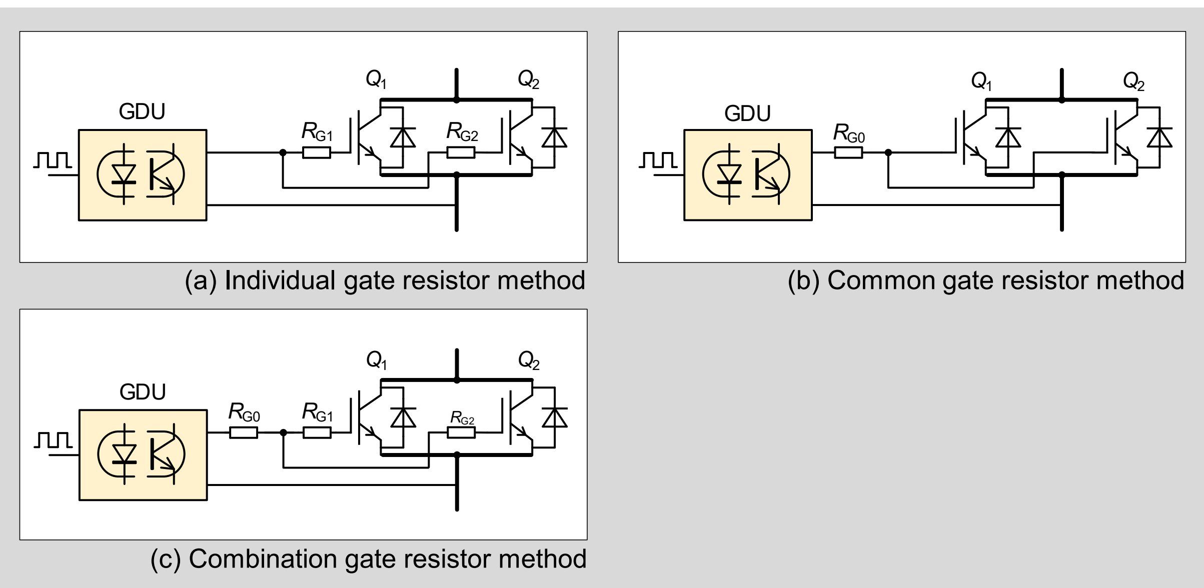

Fig. 8-9 Gate resistor configuration in common driver method

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4. Cooling Design

When connecting discrete IGBTs in parallel, it is necessary to consider the thermal interference of each IGBT. If the junction temperature T_{vj} increases due to thermal interference, the junction temperature absolute maximum rating $T_{vj(max)}$ may be exceeded and cause thermal destruction of the IGBTs. Therefore, it is necessary to consider the thermal interference between each IGBT and design the IGBTs layout to reduce T_{vj}. The points to consider regarding cooling design in parallel connection are shown below.

- Layout design considering thermal interference between each IGBT.
- Equalize cooling conditions for each IGBT.
- Uniform thermal grease thickness applied to each IGBT.

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